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T.O. 33A1-5-435-1S-1

# OPERATIONAL SUPPLEMENT
## TECHNICAL MANUAL
## OPERATION AND MAINTENANCE INSTRUCTIONS
## COUNTER, ELECTRONIC, DIGITAL READOUT
## TYPE AN/USM-326A
## BALLANTINE MODEL 9648M

Ballantine Laboratories, Inc.

THIS PUBLICATION SUPPLEMENTS T.O. 33A1-5-435-1 DATED 1 JUNE 1979.
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15 DECEMBER 1986

1. PURPOSE.

The purpose of this supplement is to amend the basic publication.

2. INSTRUCTIONS.

Section VI, page 6-11, figure 6-5 is amended as shown on page 3 of this supplement.

RADIO MAINT



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**15 MAY 1988**

1. PURPOSE.

The purpose of this supplement is to amend the basic publication.

2. INSTRUCTIONS.

PAGE 1-5

a. Section I, Paragraph 1-13., TIME BASE, subparagraph b., is amended to CHANGE Aging to read as follows:

Aging: ±3 parts in $10^9$/da averaged over 30 days after 72 hour on time following indefinite off time. (<0.2 ppm/yr)

THE END

RADIO MAINT



21

TECHNICAL MANUAL

# OPERATION AND MAINTENANCE INSTRUCTIONS

# COUNTER, ELECTRONIC, DIGITAL READOUT
# TYPE AN/USM-326A
# BALLANTINE MODEL 9648M

Ballantine Laboratories, Inc.

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# SECTION 1

# INTRODUCTION AND GENERAL INFORMATION

## 1-1. SCOPE OF MANUAL

1-2. This manual provides operation and maintenance instructions with parts breakdown for Universal Counter AN/USM-326A manufactured by Ballantine Laboratories, Inc., Boonton, New Jersey. This instrument is also identified as Ballantine Model 9648M.

1-3. Descriptive information, theory of operation, testing and troubleshooting procedures are included in this manual. Repair, replacement, and adjustment procedures are limited to those capable of being performed by organizational and intermediate level maintenance activities using tools, test equipment and spare parts authorized in the allowable list.

## 1-4. GENERAL DESCRIPTION

1-5. The AN/USM-326A, shown in Figure 1-1, is a portable, solid-state, general purpose frequency meter capable of measuring frequency directly over the range of 0.1 Hz to 550 MHz. It contains an autoranging circuit that permits time and frequency measurements to be made with automatic selection of the time base that offers optimum resolution without display overflow. Measurements are indicated on a nine digit, high intensity LED display. A twelve-position FUNCTION switch provides eleven modes of operation. There are eight manual time base ranges in decade steps from 1 us to 10 seconds and four automatic ranges that provide 6, 7, 8 or 9 digit resolution without overflow.

1-6. Universal Counter AN/USM-326A is housed in a waterproof combination case that provides explosion proofing as well as shielding from EMI. It will operate over a temperature range of from -40°C to +71°C. The detachable front cover, when installed, protects the front panel during transit or storage. The power cord and other accessories are stored in a compartment inside the front cover.

1-7. To familiarize the operator with the automatic capability of the AN/USM-326A, a comparison is made between it and the operation of a conventional, manually operated, counter-timer explaining the problems involved in measuring frequency and time interval and showing how they are solved by the AN/USM-326A.

### 1-8. FREQUENCY MEASUREMENTS (see Fig. 1-3)

In a conventional, manually operated, counter-timer, frequency measurements are performed as follows: The input signal is amplified and shaped (1) to present pulses of uniform amplitude and rise time to the decade counters (5), regardless of the frequency or waveform of the input signal. The signal gate (4) controls the flow of the shaped pulses to the decade counters. When the signal gate is enabled (opened) by a pulse from the time base dividers (3) the shaped pulses pass through and are counted by the decade counters. The next pulse from the time base chain disables (closes) the gate. The count accumulated in the decade counters is decoded (6) to convert the information into useful signals to operate the display (7). The open gate interval is divided in decade steps and is derived from the basic clock period.

With conventional frequency counters, the operator must adjust the gate time selector (time base) and make measurements at several time base frequencies until maximum resolution is seen on the readout. This method of time base selection increases the measurement time, and complicates the design of systems incorporating frequency counters. Where signals of wide frequency range are to be measured, measurements become extremely time consuming.

The autoranging feature enables the AN/USM-326A to overcome all the disadvantages of manual time base selection. The autoranging circuitry automatically adjusts the time base of the instrument so that:

a. The display capacity is never exceeded.

b. The best possible resolution is always obtained, automatically.

c. Units of measurement (kHz, MHz) are automatically displayed.

d. The decimal point is computed and placed in its correct position.

The automatic time base selection operation is concurrent with the measurement process. Thus, maximum resolution is automatically obtained and needs no attention by the operator or additional programming operations in an automatic measuring system. This increases measurement speed and simplifies system design. Signals of wide frequency range are immediately computed and displayed with maximum resolution.

### 1-9. PERIOD AND TIME INTERVAL MEASUREMENTS (see Fig. 1-4)

In a conventional, manually operated, counter-timer, period or time interval measurements are performed as follows: The input signal is applied to the amplifier and shaper (1) which converts the input signal to pulses of uniform amplitude and rise time. The shaped input signal operates a gate control circuit (2) which produces a gating pulse for the signal gate (4), equal in time to the period of the input signal. While the signal gate

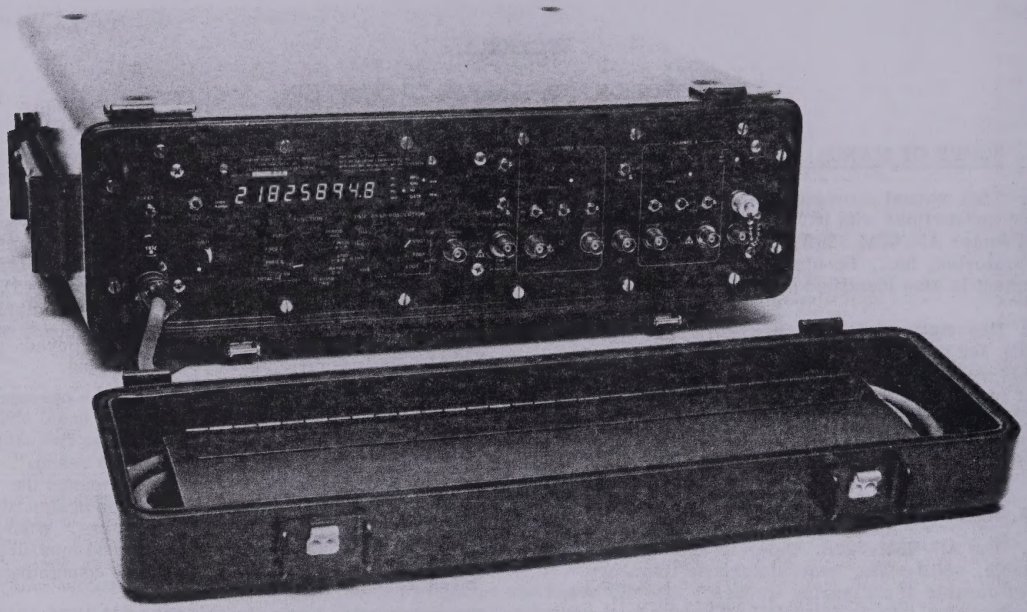


Figure 1-1. Universal Counter AN/USM-326A

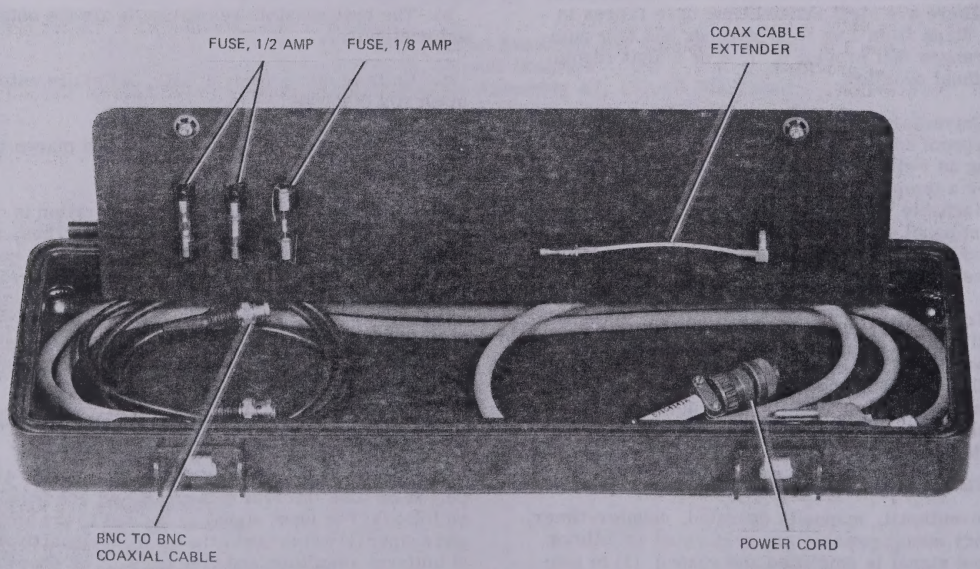


Figure 1-2. AN/USM-326A Accessories

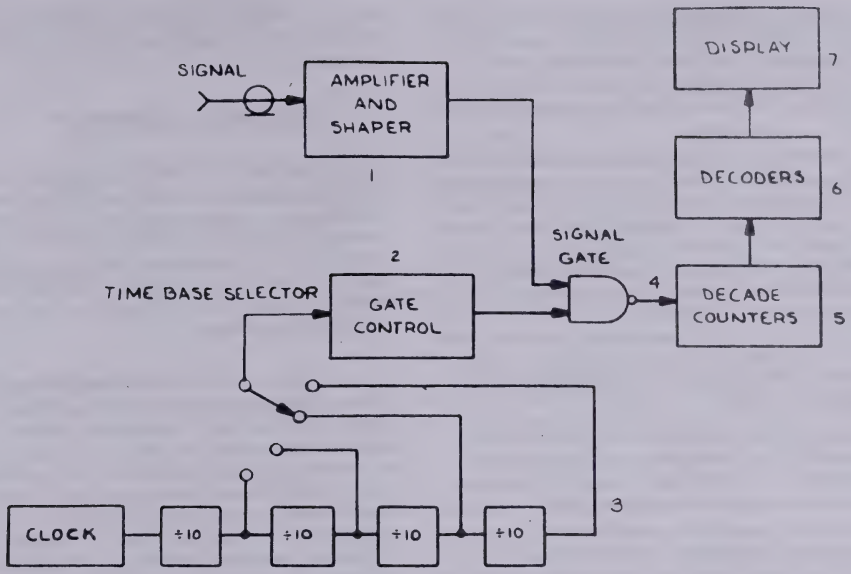


Figure 1-3. Conventional Frequency Counter Block Diagram

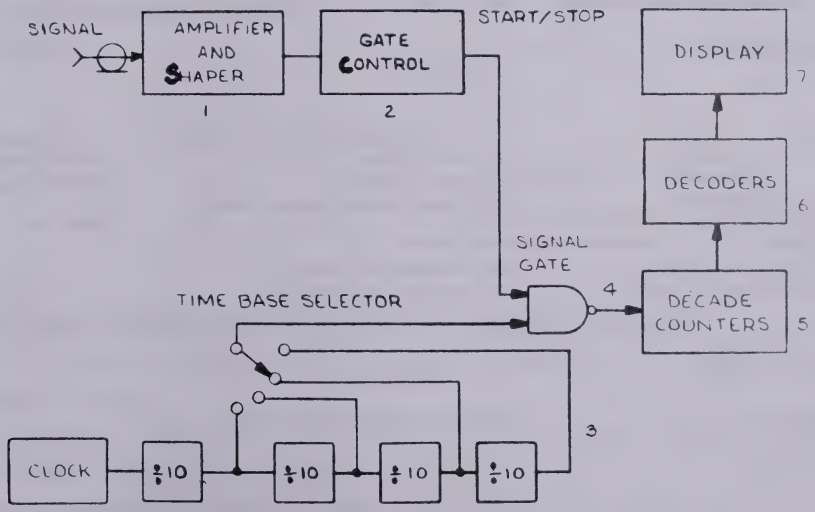


Figure 1-4. Conventional Period and Time Interval Meter Block Diagram

is enabled (open), pulses from the time base (3) pass through the signal gate to the decade counters (5). After the signal gate is closed, the count accumulated in the decade counters is decoded (6) to convert the information into useful signals to operate the display (7).

The difficulty in measuring period and time interval with the conventional method is that the operator has to know in advance the approximate duration of the signal in order to select a suitable time base (range) which will give the required resolution and prevent display overflow. If the input signal is repetitive, the operator will try to select manually, by making a few measurements, a suitable time unit for best results. However, if the input signal is non-repetitive, or the time interval to be measured is of random duration, measurements are very difficult, if not impossible, to make.

The autoranging feature enables the AN/USM-326A to overcome all the disadvantages of manual time base selection. The autoranging circuitry automatically adjusts the time base units so that:

a. The display capacity is never exceeded, except for impracticable long periods ($K \times 10^n$ seconds, where K is the lowest time unit and n the number of digits of the counter).

b. The best possible resolution is always obtained, automatically.

c. Units of measurement (microseconds, milliseconds, or seconds) are automatically displayed.

d. The decimal point is computed and placed in its correct position.

The automatic time base selection operation is concurrent with the measurement process, so that signals of random duration or duration changes are immediately computed and displayed with maximum resolution.

## 1-10. PURPOSE OF EQUIPMENT

1-11. The AN/USM-326A is a universal counter that provides a direct measurement of the frequency of signals over a range of 0.1 Hz to 550 MHz and the period of a signal from 100 ns to $10^9$ seconds. The frequency of a burst signal may be measured as easily as that of a CW signal. Special gating circuits permit the start of a measurement only when the input signal is present.

1-12. The "armed" feature enables the AN/USM-326A to have control over the exact beginning of a measurement. When armed, a separate enabling signal is applied independent of the signal to be measured. It is this signal that initiates the opening of the counting gate, not the signal being counted. This is particularly useful in applications such as the measurement of frequency variations along a frequency burst and in testing sweeper linearity by triggering the count at various voltage levels along the sweep ramp.

Single shot time interval measurements find application in time of flight (ballistic) measurements, sonar and radar ranging, navigation as well as the timing of mechanical and electromechanical (relays) devices. Provision is also made in the AN/USM-326A frequency counter for ratio, totalizing and elapsed time measurements.

## 1-13. TECHNICAL SPECIFICATIONS

### INPUT CHARACTERISTICS

a. Channel A and B

| | | |
|---|---|---|
| Coupling (A) | Switch selectable (AC, DC or LF) | Coupling (B) |
| DC coupled: | DC to 110 MHz | DC to 10 MHz |
| AC coupled: | 10 Hz to 110 MHz | 10 Hz to 10 MHz |
| LF coupled: | Attenuates signals above 1 KHz | |
| Sensitivity (A) | | (B) |
| DC to 20 MHz: | 35 mV rms (sine wave) | DC to 10 MHz: 50 mV |
| 20 MHz to 100 MHZ: | 80 mV rms (sine wave) | |

**The test limit specification remains the 80 MV RMS as required by MIL-C-87951.**

| | |
|---|---|
| Minimum Pulse Width: | 5 ns, 140 mV p-p. |
| Input Impedance: | 1 megohm shunted by <30 pF. |
| Trigger Level: | Continuously adjustable over ±2.5 volts times attenuator setting. 0 Volt preset detent is provided for simplified triggering set up. |
| Trigger Polarity: | Independent selection of + or - slope. |
| Attenuation: | X1, X10, X100 |



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Maximum Input Voltage @ 1 KHz:

| ATTENUATION | AC COUPLED | DC COUPLED |
|---|---|---|
| X1 | 500 VDC + 50V rms | 50V rms |
| X10 | 500 VDC + 150V rms | 150V rms |
| X100 | 500 VDC + 500V rms | 500V rms |

Maximum DC Blocking Voltage: ±500V

Common Input: Switch selectable; Separate A and B or Common A. In COM position sensitivity remains the same but input impedance becomes 1 MΩ paralleled by <60pF.

Dynamic Range: 35 mV to 1V rms (sine wave) X attenuator setting from 0.1 Hz to 20 MHz; 50 mV to 0.5V rms (sine wave) X attenuator setting from 20 MHz to 110 MHz.

b. Channel C

Coupling: ac coupled; ± 50V dc blocking voltage.

Sensitivity: 30 mV rms (sine wave) 30-100 MHz
15 mV rms (sine wave) 100-450 MHz
25 mV rms (sine wave) 450-550 MHz

Minimum Pulse Width: 1 ns

Input Impedance: 50Ω, nominal

Trigger Level: 0 volts

Maximum Input: 5V rms (sine wave)

Protection: Fused (1/8 A), Protects from > 5V to ≥200V.

Dynamic Range: 15 mV rms to 0.5V rms (sine wave) from 30 MHz to 550 MHz.

TIME BASE

a. Time Base Ranges

Manual: 8 decade ranges from 1μs to 10 seconds.

Automatic: 4 Autometronic resolution ranges providing full resolution without overflow of 6, 7, 8 or 9 digit display.

b. Oscillator

Hermetically sealed ovenized oscillator with proportional and fast warm-up ovens.

Frequency: 10 MHz

Aging: ±3 parts in $10^{10}$/da averaged over 30 days after 72 hour on time following indefinite off time. (<0.2 ppm/yr) see supplement 57 15 may 1978

Short term stability: ±5 parts in $10^{11}$ rms, 30 one second samples averaged over a 60 second period.

Frequency Adjustment: 2 Mechanical glass trimmer capacitors

a) Coarse 18 Turn, Range 3 x $10^{-6}$

b) Fine 18 Turn, Range 5 x $10^{-8}$

Temperature Stability: a) -40°C to 0°C: $<\pm 1$ part in $10^{10}$/°C

b) 0°C to 55°C: $<\pm 5$ parts in $10^{11}$/°C

c) 55° to 71°C: $<\pm 5$ parts in $10^{10}$/°C

Line Voltage Stability: $<\pm 1$ part in $10^{11}$ for ± 10% change in line voltage

Frequency Retrace: a) 1 hr on frequency within 2 parts in $10^9$ of 1/2 hr on frequency after being off for 24 hours.

b) After being off for 24 hours, 1 hour on frequency within 5 parts in $10^9$ of 72 hr on frequency prior to shutoff.

Fast Warm-up a) After being off 1 hour, following 4 hours of operation, frequency after 10 minutes warm up within 2 parts in $10^8$ of 4 hour on frequency.

b) After being off 4 hours, following 24 hours of operation frequency after 15 minute warm-up within 1 part in $10^8$ of 24 hour on frequency.

TOTALIZING

a. Total ON: The number of counts at the A input is totalized. The TIME BASE/RESOLUTION switch is non-functional in manual ranges. The display is limited to 6, 7, 8 or 9 digits in AUTO position.

b. Control: Totalize ON and OFF are provided by separate positions on FUNCTION switch. The display is reset with the manual RESET pushbutton on the front panel.

FREQUENCY MEASUREMENTS

a. Frequency A and B

Range (A): 0.1 Hz to 110 MHz, direct count
(B): 0.1 Hz to 10 MHz, direct count

Resolution

Manual: 1 MHz to 0.1 Hz in decade steps
Automatic: 6, 7, 8 or 9 digits with maximum resolution of 1 Hz

Accuracy: ± count ± timebase error

Display: MHz, KHz, Hz with automatically positioned decimal point

b. Frequency C

Range: 30 MHz to 550 MHz, direct count

Resolution

Manual: 1 MHz to 0.1 Hz in decade steps

Automatic: 6, 7, 8 or 9 digits with maximum resolution of 1 Hz

Accuracy: ± count ± timebase error

Display: MHz, KHz, Hz with automatically positioned decimal point

PERIOD MEASUREMENTS

a. Period A

Range: 0 to 10 MHz

| | |
|---|---|
| Resolution | |
| Manual: | 100 ns to 1 s in decade steps |
| Automatic: | 6, 7, 8 or 9 digits providing 100 ns to 1 s resolution |
| Accuracy: | ±count ± timebase error ± trigger error* |
| Display: | ns, μs, ms, sec with automatically positioned decimal point. |
| b. Period Average A | The period of the signal at Channel A input is averaged over the number of periods determined by the resolution switch (N=1 for 1μs to $10^7$ for 10 s) limited to N=$10^3$ for 6, 7, 8, 9 DGT AUTO |
| Range: | 0 to 10 MHz |
| Resolution | |
| Manual: | 1 μs to 0.1 ps in decade steps |
| Automatic: | 6, 7, 8 or 9 digits providing 1 μs to 1 ns resolution. |
| Accuracy: | ± count ± timebase error ± trigger error* Number of periods averaged |

POSITIVE/NEGATIVE PULSE WIDTH A

| | |
|---|---|
| Range: | 0 to 10 MHz |
| Resolution | |
| Manual: | 100 ns to 1 s in decade steps |
| Automatic: | 6, 7, 8 or 9 digits providing 100 ns to 1 s resolution |
| Slope Selection: | Non-functional in this mode |
| Accuracy: | ± count ± timebase error ± trigger error* |
| Display: | ns, μs, ms, sec with automatically positioned decimal point |

TIME INTERVAL A→B

| | |
|---|---|
| Range: | 100 ns to $10^9$ seconds |
| Resolution | |
| Manual: | 100 ns to 1 second in decade steps |
| Automatic: | 6, 7, 8 or 9 digits automatic with limits of 100 ns to 1 second |
| Input: | Start signal, Channel A. Stop signal, Channel B. Can be common or separate inputs |
| Accuracy: | ± count ± timebase error ± trigger error A* ± trigger error B* |
| Display: | ns, μs, ms, or SEC with automatically positioned decimal point. |

RATIO MEASUREMENTS

| | |
|---|---|
| A/B and C/B | The ratio of the frequency at A or C to the frequency at B is measured for N counts of B as selected manually by the resolution switch (N=1 for 1μs to $10^7$ for 10s) or automatically for best integral resolution of 6, 7, 8 or 9 digits. |
| Range | |
| A: | 0 to 110 MHz |
| B: | 0 to 10 MHz |
| C: | 30 to 550 MHz |
| Resolution | |
| Manual: | 1 part in $N\left(\frac{A}{B}\right)$ or $N\left(\frac{A}{C}\right)$ |
| Automatic: | 6, 7, 8 or 9 digits with 1 to 1000 averaging cycles automatically selected for maximum resolution. |
| Accuracy: | ± 1 count of A or C ± trigger error* of B X frequency of A or C when $N > 1$. For N=1, add ± 150 ns X frequency of A or C. |
| Display: | Dimensionless with automatically positioned decimal point. |

ELAPSED TIME

| | |
|---|---|
| | In the elapsed time function the internal time base is counted over the interval determined by the logic level at the ELAPSED TIME BNC connector. Digital zero, contact closure to ground or saturated transistor will enable the gate. Reset is not automatic so that any number of gated time periods will be summed in the display until manually reset. |
| Range: | 1 μs to $10^9$ seconds. |
| Resolution | |
| Manual: | 100 ns to 1 s in decade steps manually selected by the function switch. |
| Automatic: | 100 ns to 1 s in decade steps automatically selected to fill 6, 7, 8 or 9 digits of display. |

GENERAL

| | |
|---|---|
| Display: | 9 digit, high intensity, 0.43" LED display. LED decimal points and annunciators for ns, μs, ms, sec, MHz, KHz, Hz, GATE, OVN, and OVER RANGE. |
| Storage: | Holds reading between samples; switch selectable for either storage or continuously updated display. |
| Blanking: | Unwanted zeros to the left of the most significant digit are automatically suppressed except display digit locations 2 and 3. |
| Sample Rate: | Variable from < 200 ms to > 10 sec between measurements with detented HOLD position that locks display indefinitely. |
| Check Signal: | 1 MHz test signal applied to Channel A and B inputs which checks triggering, gating and logic. |
| Gate Output: | TTL level output at GATE BNC connector corresponding to the condition of the gate. High when counter gate is open. |

Marker Outputs: Channel A and B trigger output available at TTL level through individual BNC connector. Outputs may be used to identify trigger point on input signal waveform.

Arming: Switch turns arming ON or OFF. With arming ON, the measurement is armed by an input independent from the input involved in the measurement. Frequency A and Frequency C measurements are armed by an event at Channel B. The trigger slope is determined by Channel B ⌡,⌞ (slope) switch.

Environmental:

General

Complies with MIL-T-21200 Class 2 and conforms to MIL-T-28800 Type I Class 2

| Environmental Conditions | Limits | Method |
|---|---|---|
| Low Temperature, Non-Operating | -62°C | MIL-STD-810C Method 502.1 Procedure I |
| Low Temperature, Operating | -40°C | MIL-STD-810C Method 502.1 Procedure I |
| High Temperature, Non-Operating | 85°C | MIL-STD-810C Method 501.1 Procedure I |
| High Temperature, Operating | 71°C | MIL-STD-810C Method 501.1 Procedure I |
| Humidity | 95% | MIL-STD-810C Method 507.1 Procedure I |
| Altitude, Non-Operating | 40,000 ft | MIL-STD-810C Method 500.1 Procedure I |
| Altitude, Operating | 15,000 ft | MIL-STD-810C Method 500.1 Procedure I |
| Vibration | 3G | MIL-STD-810C Method 514.2 |
| Transit Drop | 26 drops | MIL-STD-810C Method 516.2 Procedure II |
| Transit Drop (Combination Case) | 14 drops | MIL-T-21200L 4.3.3.1 |
| Watertight (Combination Case) | 3 ft - 1 hr | MIL-STD-108 |
| Rain | 5 11/hr, 40 MPH | MIL-STD-810C Method 506.1 Procedure I |
| Salt Fog | 48 hr, 35°C | MIL-STD-810C Method 509 Procedure I |
| Dust | 12 hr, 63°C | MIL-STD-810C Method 510.1 Procedure I |
| Explosive Atmosphere | 15,000 ft, 55°C | MIL-STD-810C Method 511.1 Procedure I |
| Fungus Resistance | Waived - No fungus nutrient materials used | |

Electromagnetic Compatibility:

General

Complies with MIL-T-21200 Class 2 and conforms to MIL-T-28800 Type I Class 2

Tests in accordance with MIL-STD-461

CE01
CE03
CS01
CS02
CS06
RE02 Tested to 10 GHz in excess of requirements
RS02
RS03

Power Requirements: 100/120/220/240V rms ± 10% (switch selectable), 50 to 400 Hz ± 5%, 95VA Max.

Dimensions

Height: 136.5 mm. (5 3/8 in.)

Width: 482.6 mm. (19 in.)

Depth: 482.6 mm. (19 in.)

Weight:

| | |
|---|---|
| Accessories Furnished: | Fuse, 1/2 A (2) P/N 19-03411-OA<br>Fuse, 1/8A P/N 19-10006-OA<br>Power Cord P/N 89-10414-1A<br>50Ω, 4 ft, BNC to BNC Coaxial Cable, P/N 88-10045-1A<br>Instruction Manual P/N<br>Circuit Board Extender, 40 Pin P/N 89-10862-1A<br>Circuit Board Extender, 26 Pin P/N 89-10863-1A<br>Coax Cable Extender P/N 88-10039-1B |
| Options Available | |
| Option 36: | Extends frequency of Channel C to 1.25 GHz. |
| Option 60: | IEEE - 488 Bus Interface |

*Trigger error is <0.3% of one period for sinewaves having signal to noise ratio of 40 dB or better and amplitude equal to the sensitivity of the counter. For any wave shape the trigger error is less than:

$$\frac{\pm 2 \times \text{Peak Noise Voltage}}{\text{Signal Slope}} \quad \text{or} \quad \frac{\pm 0.0025\ \mu s}{\text{Signal Slope (V/}\mu s\text{)}}$$

## SECTION II

## INSTALLATION

### 2-1. UNPACKING AND INITIAL INSPECTION

2-2. The AN/USM-326A requires no special preparation prior to using. This section contains unpacking, inspection, and installation information.

2-3. Examine the shipping carton for damage before unpacking the instrument. Carefully remove it from the carton and check immediately for any shipping damage such as dents or loose parts. Remove the front cover by unfastening the two latches located at the bottom front of the instrument. Open it fully and slide it to the right until free of the hinge pins. Check the items received against the list of accessories.

### 2-4. POWER REQUIREMENTS

2-5. The AN/USM-326A is designed to operate from a power source of 100/120/220 or 240V rms ±10% and, 50 to 400 Hz ±5% power source. The primary voltage selection is made by a four position rotary switch located on the front panel.

CAUTION

Prior to operating this switch, make sure that the power cord is disconnected or the instrument might be damaged. Determine the correct power source available, then switch the line voltage selector to the applicable position.

WARNING

This equipment is provided with a three-conductor power cord which will ground the case when connected to a three-connector outlet. If a grounded outlet is not available, an adapter must be used which provides a good ground connection.

2-6. Remove the power cable from its storage inside the front cover. Connect the cable to the front panel AC Power Receptacle.

### 2-7. INSTALLATION REQUIREMENTS

2-8. Locate the AN/USM-326A in a position that provides adequate clearance on all sides so that heat may be dissipated. Be sure that this permits sufficient air circulation and that nearby equipment does not discharge hot air directly on the instrument. The outline and mounting dimensions are shown in Figure 2-1.

2-9. Connect the power cable to an appropriate receptacle. The instrument is now ready for use.

2-10. Check the operation of the AN/USM-326A by referring to the performance checks in Section III. For a complete performance assurance test see Section V.

### 2-11. PREPARATION FOR RESHIPMENT AND STORAGE

2-12. If the instrument is to be shipped or stored for long periods of time, repackage the unit as described in the following procedure and as shown in Figure 2-2. Use either the original packing material, if available, or material similar to that specified.

a. Disconnect the power cable and stow it in the front cover storage compartment.

b. Attach the front cover to the case and secure it by fastening the two latches.

c. Package the unit using U.S. Government method IIC.

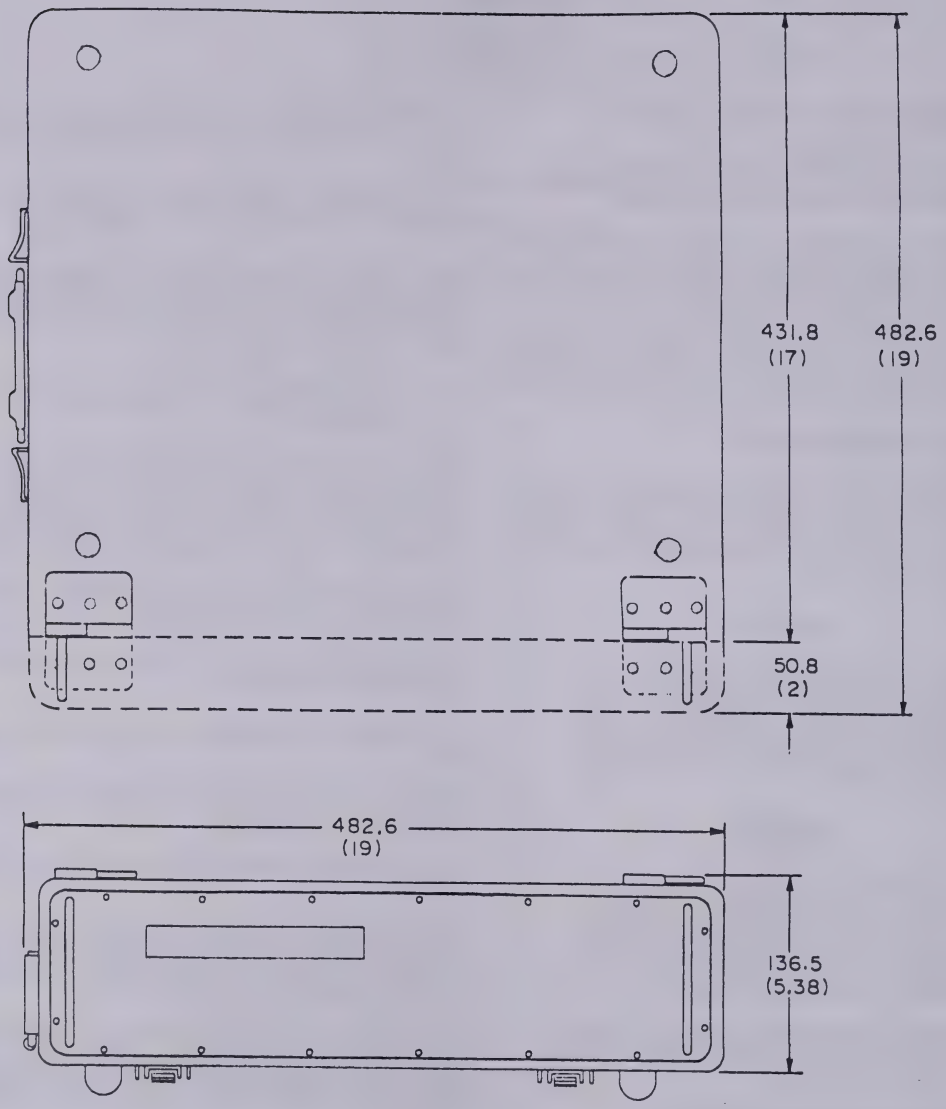
d. Tape a 4 unit bag of desiccant (MIL-D-3464) at the rear of the instrument.

e. Enclose the instrument in a plastic bag and seal the bag.

f. Wrap the covered unit in 1" thick, flexible, cellular, plastic film cushioning material (PPP-C-795) and place in a barrier bag (MIL-B-131). Extract the air from the bag and heat seal.

g. Place the bagged instrument in a fiberboard box (PPP-B-636) of suitable size. Fill the spaces with rubberized hair or cellular plastic cushioning material. Close the box and seal with 2" wide, water-resistant, cloth tape.

h. Mark the carton "FRAGILE," "HANDLE WITH CARE," or similar precautionary notice. If required, affix shipping labels or mark the carton to identify the contents in accordance with MIL-STD-129.




NOTE: ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES).

Figure 2-1. AN/USM-326A Outline Drawing

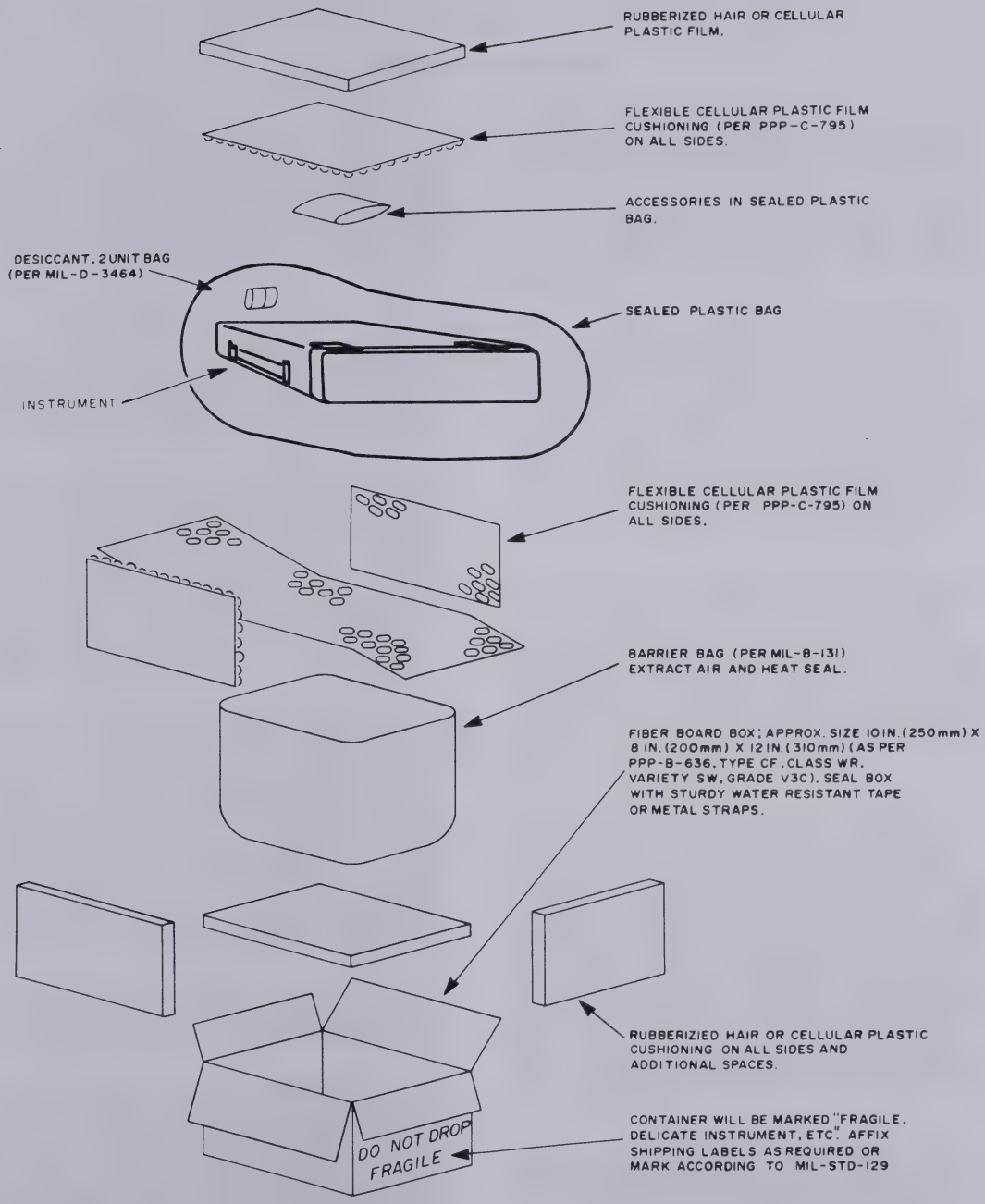

RUBBERIZED HAIR OR CELLULAR PLASTIC FILM.
FLEXIBLE CELLULAR PLASTIC FILM CUSHIONING (PER PPP-C-795) ON ALL SIDES.
ACCESSORIES IN SEALED PLASTIC BAG.
DESICCANT, 2 UNIT BAG (PER MIL-D-3464)
SEALED PLASTIC BAG
INSTRUMENT
FLEXIBLE CELLULAR PLASTIC FILM CUSHIONING (PER PPP-C-795) ON ALL SIDES.
BARRIER BAG (PER MIL-B-131) EXTRACT AIR AND HEAT SEAL.
FIBER BOARD BOX; APPROX. SIZE 10 IN. (250mm) X 8 IN. (200mm) X 12 IN. (310mm) (AS PER PPP-B-636, TYPE CF, CLASS WR, VARIETY SW, GRADE V3C). SEAL BOX WITH STURDY WATER RESISTANT TAPE OR METAL STRAPS.
RUBBERIZIED HAIR OR CELLULAR PLASTIC CUSHIONING ON ALL SIDES AND ADDITIONAL SPACES.
DO NOT DROP
FRAGILE
CONTAINER WILL BE MARKED "FRAGILE, DELICATE INSTRUMENT, ETC." AFFIX SHIPPING LABELS AS REQUIRED OR MARK ACCORDING TO MIL-STD-129

Figure 2-2. AN/USM-326A Packing Diagram

# SECTION III

# OPERATING INSTRUCTIONS

## 3-1. INTRODUCTION

3-2. This section contains operating instructions for the AN/USM-326A Counter-Timer as well as an explanation of the controls, indicators, and connectors. Detailed performance test procedures, troubleshooting, and calibration procedures are included in Section V.

## 3-3. OPERATING MODES

3-3-1. General. The AN/USM-326A has eleven operating modes. The operating modes are TOTAL, FREQ A, FREQ C, PERIOD, ⎍ (Positive Pulsewidth), ⎎ (Negative Pulsewidth), PERIOD AVG, T INTVL A→B, RATIO A/B, RATIO C/B and ELAPSED TIME.

3-3-2. TOTAL Mode. In the TOTAL mode, the signal gate is manually controlled. The gate is initially disabled by rotating the FUNCTION switch to the TOTAL OFF position. Any count in the display is then cleared by depressing the RESET switch. When the FUNCTION switch is operated to the TOTAL ON position, a signal applied to Channel A will be continuously totalized until the switch is rotated back to the OFF position or the number of events exceeds the capacity of the decade counters, at which time the OVER RANGE lamp will light.

3-3-3. FREQUENCY A Mode. Frequency can be measured with a signal input to Channel A (0.1 to 110 MHz). In the FREQ A mode the number of input signal voltage transitions through the trigger point of the counter is measured over a single gate period selected by the TIME BASE/RESOLUTION SWITCH, The gate is variable in decade steps from 1 us to 10 s and can be manually selected for desired resolution. To optimize the choice of time base the instrument features automatic time base selection based on setting the RESOLUTION to 6, 7, 8, or 9 digits. Table 3-1 lists the automatic resolution positions and gives the corresponding readouts for a range of input frequencies.

3-3-4. FREQUENCY C Mode. Same function as the FREQUENCY A mode except the signal input is applied to CHANNEL C. (For frequencies between 30 and 550 MHz).

3-3-5. PERIOD Mode. In the PERIOD mode, the period of a signal applied to the Channel A input connector is measured by counting the pulses produced by the internal time base over a single period of the input signal. The time base is manually or automatically selected to provide the maximum resolution for the applied signal. The maximum number of digits automatically displayed is variable from 6 to 9 by the TIME BASE/RESOLUTION switch. Table 3-2 lists the positions of this switch and gives the corresponding readouts for a range of input frequencies.

3-3-6. ⎍, ⎎ (Positive and Negative Pulsewidth modes.) In the ⎍ Positive Pulsewidth and ⎎ Negative Pulsewidth modes, the pulses produced by the internal time base are counted over the period of the input signal.

3-3-7. PERIOD AVG Mode. In the PERIOD AVG mode, the average period of a signal applied to the INPUT A connector is measured by counting the pulses produced by the internal time base over from 1 to $10^7$ manually selected or 1 to $10^3$ automatically selected periods of the input signal. The number of periods averaged may be automatically selected to provide maximum resolution for the applied signal. Table 3-3 gives the seven-digit display readout, and the number of periods over which the frequency is averaged, for a range of input frequencies.

3-3-8. T INTVL A→B Mode. In the T INTVL A→B mode, the pulses produced by the internal time base are counted over the interval between the initiation of a start pulse to the Channel A amplifier and the initiation of a stop pulse to the Channel B amplifier. One application for the T INTVL A→B mode is the measurement of elapsed time between two signals. The T INTVL A→B mode can also be used to measure the elapsed time between two selected points on a single waveform.

3-3-9. RATIO A/B Mode. In the RATIO A/B mode, the ratio of two frequencies can be measured directly. One frequency is applied to the INPUT A connector and the source of the other frequency is applied to the INPUT B connector. Both connectors are located on the front panel. The measurement is made by counting the number of A pulses occurring in 1 to $10^7$ manually selected or 1 to $10^3$ automatically selected periods of B. The number of periods over which the A pulses are counted may be selected automatically to provide maximum resolution. The a readout is the ratio of frequency A to frequency B with automatic positioning of the decimal point. The frequency limits of the A and B inputs must be observed.

3-3-10. RATIO C/B Mode. Same function as the RATIO A/B mode except of one frequency is applied to the INPUT C connect or instead of the INPUT A connector. The frequency limits of C input must be observed.

3-3-11. ELAPSED TIME Mode. In the ELAPSED TIME mode, the pulses produced by the internal time base are counted over the interval determined by the remote count-enable input applied to the ELAPSED TIME BNC connector. Counting is enabled when the input is a TTL logic 0 and is inhibited when the input is a TTL logic 1. Resetting is not automatic in the ELAPSED TIME mode. Unless the instrument is reset manually, the value obtained in the first interval will be stored and will add to the count obtained in subsequent intervals.

## 3-4. CONTROLS, INDICATORS, AND CONNECTORS

3-5. The operating controls, indicators, and connectors located on the front panel of the AN/USM-326A are shown in Figure 3-1. The front panel functions described in Table 3-4.

Table 3-1. Frequency Measurement Display

| INPUT SIGNAL FREQUENCY | AUTO RESOLUTION | | | |
|---|---|---|---|---|
| | 6 DGT | 7 DGT | 8 DGT | 9 DGT |
| 10 Hz | .010 kHz | 0.010 kHz | 0.010 kHz | 0.010 kHz |
| 100 Hz | 0.100 kHz | 0.100 kHz | 0.100 kHz | 0.100 kHz |
| 1 kHz | 1.000 kHz | 1.000 kHz | 1.000 kHz | 1.000 kHz |
| 10 kHz | 10.000 kHz | 10.000 kHz | 10.000 kHz | 10.000 kHz |
| 100 kHz | 100.000 kHz | 100.000 kHz | 100.000 kHz | 100.000 kHz |
| 1 MHz | 1.00000 MHz | 1000.000 kHz | 1000.000 kHz | 1000.000 kHz |
| 10 MHz | 10.0000 MHz | 10.00000 MHz | 10000.000 kHz | 10000.000 kHz |
| 100 MHz | 100.000 MHz | 100.0000 MHz | 100.00000 MHz | 100000.000 kHz |

Table 3-2. Period Measurement Display

| INPUT SIGNAL PERIOD | AUTO RESOLUTION | | | |
|---|---|---|---|---|
| | 6 DGT | 7 DGT | 8 DGT | 9 DGT |
| 10 sec | 10000.0 ms | 10000.00 ms | 10000.000 ms | 10000000.0 us |
| 1 sec | 1000.00 ms | 1000.000 ms | 1000000.0 us | 1000000.0 us |
| 100 ms | 100.000 ms | 100000.0 us | 100000.0 us | 100000.0 us |
| 10 ms | 10000.0 us | 10000.0 us | 10000.0 us | 10000.0 us |
| 1 ms | 1000.0 us | 1000.0 us | 1000.0 us | 1000.0 us |
| 100 us | 100.0 us | 100.0 us | 100.0 us | 100.0 us |
| 10 us | 10.0 us | 10.0 us | 10.0 us | 10.0 us |
| 1 us | 1.0 us | 1.0 us | 1.0 us | 1.0 us |

Table 3-3. Period Average Measurement Display

| INPUT SIGNAL PERIOD | 7 DGT AUTO RESOLUTION | |
|---|---|---|
| | NO. OF PERIODS AVERAGED | READOUT |
| 1 sec | 1 | 1000000 us |
| 100 ms | 10 | 100000.0 us |
| 10 ms | 100 | 10000.00 us |
| 1 ms | 1000 | 1000.000 us |
| 100 us | 1000 | 100.000 us |
| 10 us | 1000 | 10.000 us |
| 1 us | 1000 | 1.000 us |

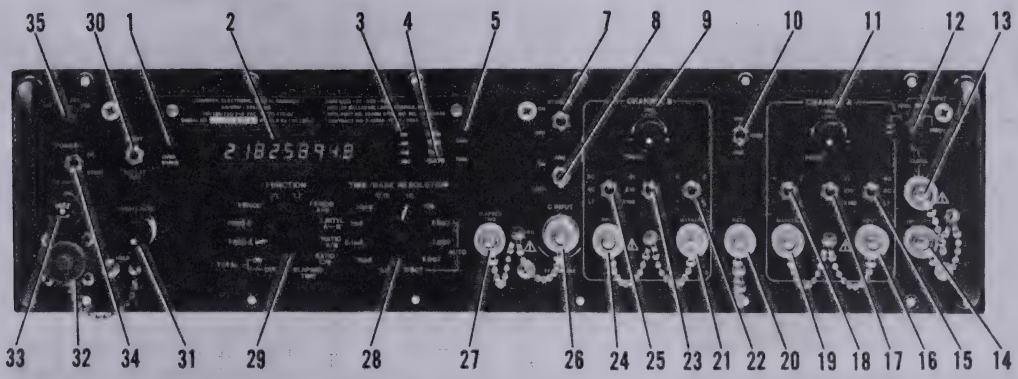



Figure 3-1. AN/USM-326A Front Panel Controls, Indicators, and Connectors

Table 3-4. Controls, Indicators and Connectors

| INDEX NO. | CONTROL INDICATOR OR CONNECTOR | REFER. DESIG. | FUNCTION |
|---|---|---|---|
| 1 | OVER RANGE Indicator | | Indicator lamp that illuminates when the display range is exceeded. |
| 2 | Display | | A 9-digit numeric readout with automatically positioned decimal point that indicates the magnitude of the quantity measured. |
| 3 | Units of measurement Indicators | | Units for the readout are shown by indicators to the right of the display. (ns, us, ms, sec, Hz, kHz, and MHz). |
| 4 | GATE Indicator | | Indicator lamp that illuminates when the instrument is counting. |
| 5 | OVN Indicator | | Indicator lamp that illuminates when the power cord is plugged in (regardless of the POWER switch position) indicating that power is applied to the crystal oven circuits. |
| 6 | REM Indicator | | Remote program indicator lamp. Used only with IEEE - 488 Bus Interface (Option 60). |
| 7 | STORAGE Switch | | A two-position toggle switch that when ON, provides storage of previous display reading while new measurement is made. In the OFF position, the display is continuously updated. |
| 8 | ARM Switch | | A two-position toggle switch that selects armed operation of either Channel A or C through Channel B input when in the ON position and normal operation in OFF position. |
| 9 | Channel B TRIG LEVEL | | A potentiometer that varies the triggering level of the input amplifier by the input waveform. When the control is turned fully counter-clockwise to the detented PRESET position, a preset 0 volt trigger level provides easy trigger set-up for symmetrical-to-ground waveforms. |
| 10 | SEP-COM-CHK Switch | | A three-position toggle switch that connects Channel A and Channel B input circuits to a common input connector (input A) in the COM position or to separate connectors in the SEP position. In the CHK position, an internal 1 MHz test signal is applied simultaneously to both Channels. |

Table 3-4. Controls, Indicators, and Connectors (Cont)

| INDEX NO. | CONTROL, INDICATOR OR CONNECTOR | REFER. DESIG. | FUNCTION |
|---|---|---|---|
| 11 | Channel A TRIG LEVEL Control | | Same function as Channel B TRIG LEVEL control. |
| 12 | INT OUT, EXT INPUT Switch | | A four-position, screwdriver actuated, rotary switch that selects either an internal 10 MHz clock output or any of three external frequency standard inputs. (1 MHz, 5 MHz, 10 MHz). |
| 13 | CLOCK Connector | | BNC connector providing external frequency standard input or 10 MHz internal clock output. |
| 14 | 1 MHz OUT Connector | | BNC connector providing a continuous 1 MHz sinewave output whose stability is referenced to the internal oscillator. |
| 15 | Channel A DC, AC, LF Switch | | A three-position toggle switch that selects AC coupling, DC coupling or attenuates signals above 1 kHz in the LF position. |
| 16 | Channel A INPUT Connector | | BNC signal input connector. High impedance. |
| 17 | Channel A X1, X10, X100 Switch | | A three-position toggle switch that varies the attenuation (X1, X10, X100) of the signal applied to the Channel A connector. |
| 18 | Channel A ⌐ , ⌙ (Slope) Switch | | A two-position toggle switch that permits triggering on either positive (⌐) or negative (⌙) edges of a signal applied to Channel A in the PERIOD, PERIOD AVG, and T INTVL A→B modes. |
| 19 | Channel A MARKER Connector | | BNC connector for Channel A trigger point signal output. |
| 20 | GATE Output Connector | | BNC connector for counter gate signal output. |
| 21 | Channel B MARKER Connector | | BNC connector for Channel B trigger point signal output. |
| 22 | Channel B ⌐ , ⌙ (Slope) Switch | | Same function as Channel A ⌐, ⌙ Switch. |
| 23 | Channel B X1, X10, X100 Switch | | Same function as Channel A X1, X10, X100 Switch. |
| 24 | Channel B INPUT Connector | | BNC signal input connector. High impedance. |
| 25 | Channel B DC, AC, LF Switch | | Same function as Channel A DC, AC, LF Switch. |

Table 3-4. Controls, Indicators, and Connectors (Cont)

| INDEX NO. | CONTROL, INDICATOR OR CONNECTOR | REFER. DESIG. | FUNCTION |
|---|---|---|---|
| 26 | Channel C INPUT Connector | | Fused (1/8 A) input connector. 50 Ω impedance. |
| 27 | ELAPSED TIME Connector | | BNC connector. Contact closure to ground or saturated transistor (TTL Zero) enables counting in the ELAPSED TIME mode. |
| 28 | TIME BASE/RESOLUTION Switch | | A 12-position rotary switch that selects the time base manually or the number of digits to be automatically displayed (resolution). |
| 29 | FUNCTION Switch | | A 12-position rotary switch that selects any of eleven measurement modes. |
| 30 | RESET/DISPLAY TEST Pushbutton | | Resets both the display and internal count to zero. Also checks display by lighting all segments. |
| 31 | SAMPLE RATE/HOLD Control | | A potentiometer that varies the rate at which the display samples (independent of the gate time). When the control is turned fully counterclockwise to the detented HOLD position, the display is held indefinitely. |
| 32 | AC Power Receptacle | | MS3102A10L-3p type power input connector with third pin connected to instrument case for earth ground connection. |
| 33 | Fuse (1/2 AMP SB) | | Protects primary power input circuit from accidental overload. |
| 34 | POWER Switch | | A two-position toggle switch that applies AC power to the instrument in the ON position. In the STDBY position, power is supplied only to the crystal oven whenever the power cord is plugged in. |
| 35 | 100, 120, 220, 240 Switch | | A four-position, screwdriver actuated, rotary switch that permits selection of the correct power transformer primary connections compatible with 100/120/220/240V rms mains operation.<br><br>CAUTION<br><br>This switch should be pre-set to the proper available mains voltage before plugging the power cord in. Never operate the switch without first disconnecting the power cord. |

## 3-6. PERFORMANCE CHECKS

3-7. The performance of the AN/USM-326A should be checked upon initial receipt, before each usage and after maintenance has been performed.

3-8. The AN/USM-326A has an internal test circuit that provides a confidence check of the instrument's operation. This checkout is performed by the following procedure:

3-8-1. Set the SEP-COM-CHK switch to the CHK position.

3-8-2. Set Channel A and Channel B TRIG LEVEL controls to PRESET.

3-8-3. Rotate the FUNCTION switch to TOTAL OFF and TIME BASE/RESOLUTION switch to 1s.

3-8-4. Check that when RESET push-button is depressed, all 9 digits read "8" for DISPLAY TEST.

3-8-5. Check that when RESET push-button is released, the 3 least significant digits read "0" and that all other digits are extinguished.

3-8-6. Set the TIME BASE/RESOLUTION switch to the 6DGT position and then rotate the FUNCTION switch to the TOTAL ON position. Check that the GATE annunciator lights. Check that the OVER RANGE annunciator lights when the count exceeds 999999.

3-8-7. Rotate the TIME BASE/RESOLUTION control to 7DGT. Push RESET. Check that the GATE annunciator lights. Check that the OVER RANGE annunciator lights when the count exceeds 9999999.

3-8-8. Perform the same check as in step 7 but with the TIME BASE/RESOLUTION control set to 8DGT. The OVER RANGE annunciator should light when the count exceeds 99999999.

3-8-9. Set the FUNCTION switch to TOTAL OFF. Check that the GATE lamp extinguishes and that the display is held.

3-8-10. Rotate the FUNCTION switch to FREQ A. Set the STORAGE switch to ON and turn the SAMPLE RATE control fully clockwise. The display should indicate frequency in accordance with Table 3-5.

3-8-11. Rotate the FUNCTION switch to FREQ C. Set the STORAGE switch to ON and turn the SAMPLE RATE control fully clockwise. Check that INT OUT, EXT INPUT switch is in INT OUT position. Connect BNC to BNC coax cable from CLOCK BNC connector to C INPUT BNC connector. The display should indicate frequency in accordance with Table 3-6.

3-8-12. Rotate the FUNCTION switch to PERIOD. The display should indicate period in accordance with Table 3-7.

3-8-13. Rotate the FUNCTION switch to ⎍ Positive Pulsewidth. The display should indicate in accordance with Table 3-8.

3-8-14. Rotate the FUNCTION switch to ⎏ Negative Pulsewidth. The display should indicate in accordance with Table 3-8.

3-8-15. Rotate the FUNCTION switch to PERIOD AVG. The display should indicate in accordance with Table 3-9.

3-8-16. Rotate the FUNCTION switch to T INTVL A→B. The display should indicate in accordance with Table 3-7 if the slope switches of Channel A and Channel B are both set to + position or if they are both set to the - position. If either slope switch is set to the opposite polarity of the other, the display should indicate in accordance with Table 3-8.

3-8-17. Rotate the FUNCTION switch to RATIO A/B position. The display should indicate in accordance with Table 3-10.

3-8-18. Rotate the FUNCTION switch to the ELAPSED TIME position and set the TIME BASE/RESOLUTION switch to 10s. Reset the count to zero. Enable the counting by shorting the center of the ELAPSED TIME BNC Connector to its shell (ground). The display should count continuously, in seconds, for the duration the count is enabled. When the count is disabled, the display should indicate the total time elapsed.

## 3-9. INPUT CONTROL ADJUSTMENT

The input controls for both Channel A and Channel B are identical. The correct setting of these controls is of prime importance in order to obtain the best possible results. The choice of AC or DC coupling depends on the type of signal to be measured. If the signal has a small AC component riding on a DC level, AC coupling should be used. For symmetrical signals, AC coupling is desirable. For very asymmetrical signals, such as pulses with low-duty cycle, DC coupling is preferable, particularly if the pulses are random. For waveforms below 1 kHz, the coupling selector switch should be set to LF. This position attenuates signals above 1 kHz and will filter out noise superimposed on the input waveform. Never use the LF position when the desired input signal has higher frequency components. Attenuation should be selected as required: X1 (±2.5 volt), X10 (±25 volts) or X100 (±250 volts). If the input signal is not known, begin with X100 attenuation and decrease as required.

The ⎍ , ⎏ (slope) switch selects whether the instrument triggers on the positive or negative going edge of the input waveform. For sinusoidal waveforms, the choice is usually arbitrary, but for other waveforms it is desirable to trigger on the steepest slope in order to minimize trigger error.

The TRIG LEVEL control sets the triggering point on the input waveform at any level between +2.5 and -2.5

volts. For input signals that cross ground level, the trigger level can be preset at zero cross over (PRESET). For the correct input circuit adjustment proceed as follows:

a. Set the FUNCTION switch to TOTAL ON.

b. Connect a signal to the Channel A INPUT BNC connector.

c. Set the DC, AC, LF and ⎍ , ⎏ (slope) switches as explained previously.

d. Set X1, X10, X100 switch to X100 and rotate the Channel A TRIG LEVEL control from fully counterclockwise to fully clockwise observing the points at which the counting stops. Decrease attenuation until proper counting is obtained through an angle of rotation of the TRIG LEVEL control of approximately 15 degrees.

e. Set the TRIG LEVEL control midway between the 15-degree angle. During adjustment, the point of the waveform at which the counter is triggered may be observed on a high-input impedance oscilloscope connected to the MARKER Output BNC.

The B Channel should be adjusted in the same way but in place of the display, an oscilloscope connected to the MARKER B Output BNC should be used for the correct count observation.

NOTE

To minimize interchannel crosstalk due to high-amplitude input signals in the T INTVL A→B and A/B modes of operation, a low-impedance termination (50 ohms) should be connected to the BNC input connectors. Otherwise, the input signals should be attenuated before application to the counter inputs. Input C is a 50 ohm input. Use this input when measuring FREQ C in the range of 30 MHz to 550 MHz. DO NOT exceed 50V dc or 5V rms (sine wave) or 200 volt peak pulse voltages. A 1/8 ampere fuse located in the Channel C input BNC connector will protect Channel "C" from damage by ac inputs above 5V rms (sine wave).

## 3-10. OPERATING PROCEDURE

3-11. Figures 3-2 through 3-11 describe typical operating procedures.

Table 3-5. Frequency A

| TIME BASE/ RESOLUTION | DISPLAY RDG. ± 1 COUNT | TIME BASE/ RESOLUTION | DISPLAY RDG. ± 1 COUNT |
|---|---|---|---|
| 1 us | 001 MHz | 1 s | 1000000 Hz |
| 10 us | 01.0 MHz | 10 s | 1000000.0 Hz |
| 0.1 ms | 1.00 MHz | 6 DGT | 1.00000 MHz |
| 1 ms | 1.000 MHz | 7 DGT | 1000.000 kHz |
| 10 ms | 1000.0 kHz | 8 DGT | 1000.000 kHz |
| 0.1 s | 1000.00 kHz | 9 DGT | 1000.000 kHz |

Table 3-6. Frequency C

| TIME BASE/ RESOLUTION | DISPLAY RDG. 1 COUNT | TIME BASE/ RESOLUTION | DISPLAY RDG. 1 COUNT |
|---|---|---|---|
| 1 us | 010 MHz | 1 s | 10000000 Hz |
| 10 us | 10.0 MHz | 10 s | 10000000.0 Hz |
| 0.1 ms | 10.00 MHz | 6 DGT | 10.0000 MHz |
| 1 ms | 10.000 MHz | 7 DGT | 10.00000 MHz |
| 10 ms | 10000.0 kHz | 8 DGT | 10000.000 kHz |
| 0.1 s | 10000.00 kHz | 9 DGT | 10000.000 kHz |

Table 3-7. Period

| TIME BASE/ RESOLUTION | DISPLAY RDG. ± 1 COUNT | TIME BASE/ RESOLUTION | DISPLAY RDG. ±1 COUNT |
|---|---|---|---|
| 1 us | 01.0 us | 1 s | 00.0 s |
| 10 us | .001 ms | 10 s | 000 s |
| 0.1 ms | 0.00 ms | 6 DGT | 01.0 us |
| 1 ms | 00.0 ms | 7 DGT | 01.0 us |
| 10 ms | .000 s | 8 DGT | 01.0 us |
| 0.1 s | 0.00 s | 9 DGT | 01.0 us |

Table 3-8. Pulsewidth

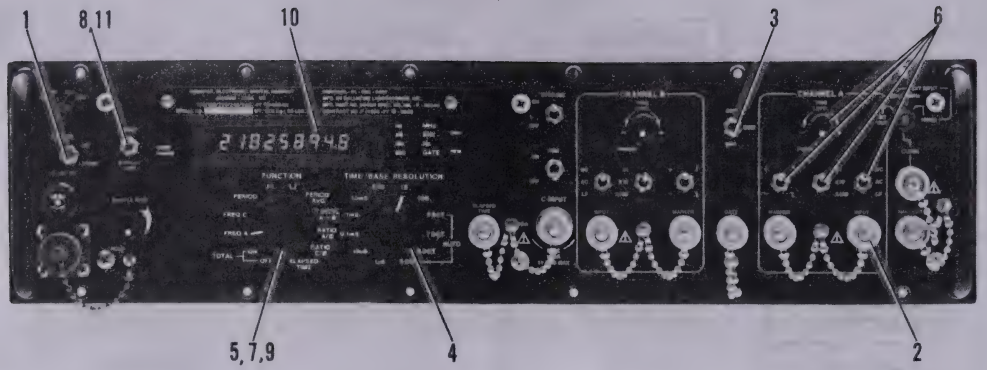
| TIME BASE/ RESOLUTION | DISPLAY RDG. ± COUNT |
|---|---|
| 1 us | 00.5 us |
| 6 DGT | 00.5 us |
| 7 DGT | 00.5 us |
| 8 DGT | 00.5 us |
| 9 DGT | 00.5 us |

Table 3-9. Period Average

| TIME BASE/ RESOLUTION | DISPLAY RDG. ± 1 COUNT | TIME BASE/ RESOLUTION | DISPLAY RDG. ± 1 COUNT |
|---|---|---|---|
| 1 us | 001 us | 1 s | 1000.000 ns |
| 10 us | 01.0 us | 10 s | 1000.0000 ns |
| 0.1 ms | 1.00 us | 6 DGT | 1.000 us |
| 1 ms | 1.000 us | 7 DGT | 1.000 us |
| 10 ms | 1000.0 ns | 8 DGT | 1.000 us |
| 0.1 s | 1000.00 ns | 9 DGT | 1.000 us |

Table 3-10. Ratio A/B

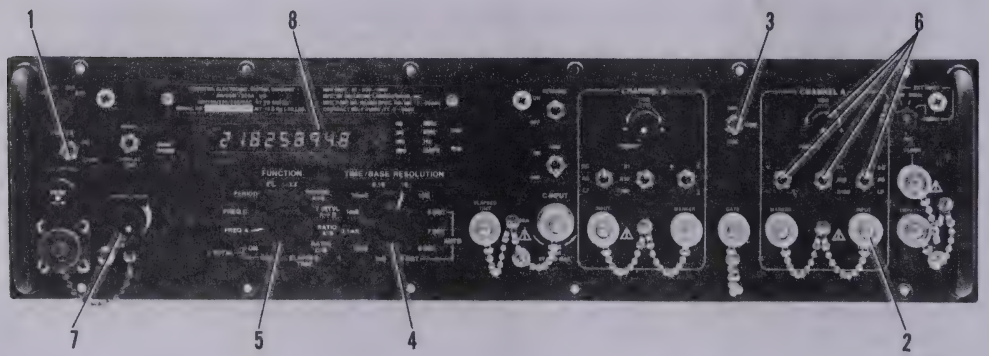
| TIME BASE/ RESOLUTION | DISPLAY RDG. ± 1 COUNT | TIME BASE/ RESOLUTION | DISPLAY RDG. ± 1 COUNT |
|---|---|---|---|
| 1 us | 001 | 1 s | 1.000000 |
| 10 us | 01.0 | 10 s | 1.0000000 |
| 0.1 ms | 1.00 | 6 DGT | 1.000 |
| 1 ms | 1.000 | 7 DGT | 1.000 |
| 10 ms | 1.0000 | 8 DGT | 1.000 |
| 0.1 s | 1.00000 | 9 DGT | 1.000 |




1. Turn POWER switch ON.
2. Connect signal to be counted to Channel A INPUT connector.
3. Set SEP-COM-CHK switch to SEP.
4. Set TIME BASE/RESOLUTION switch to 1 us.
5. Set FUNCTION switch to TOTAL ON.
6. Adjust Channel A input circuit as outlined in paragraph 3-9.
7. Set FUNCTION switch to TOTAL OFF.
8. Press RESET pushbutton.
9. Start the count by setting the FUNCTION switch to TOTAL ON and stop by setting to TOTAL OFF.

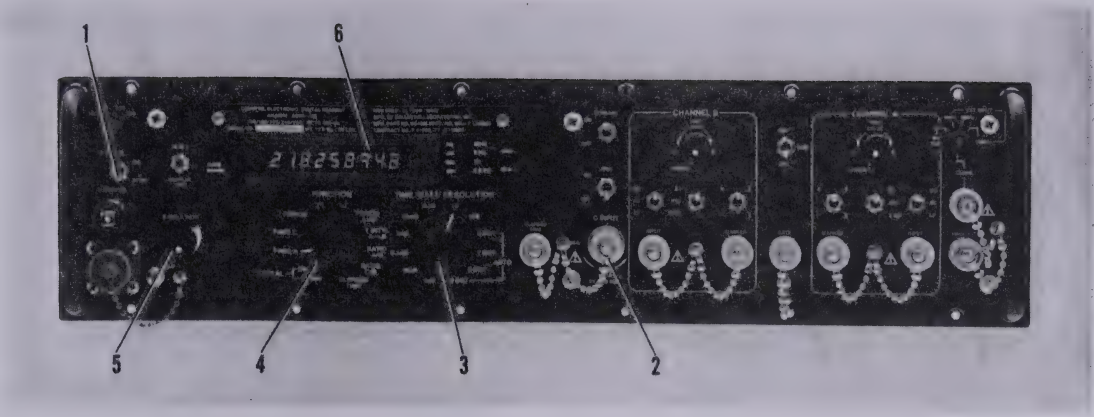
   NOTE: If the OVER RANGE indicator lights, the indicated display is NOT the total count.
10. The display will indicate the total count.
11. Return the display to zero by pressing RESET.

Figure 3-2. Operation in TOTAL mode



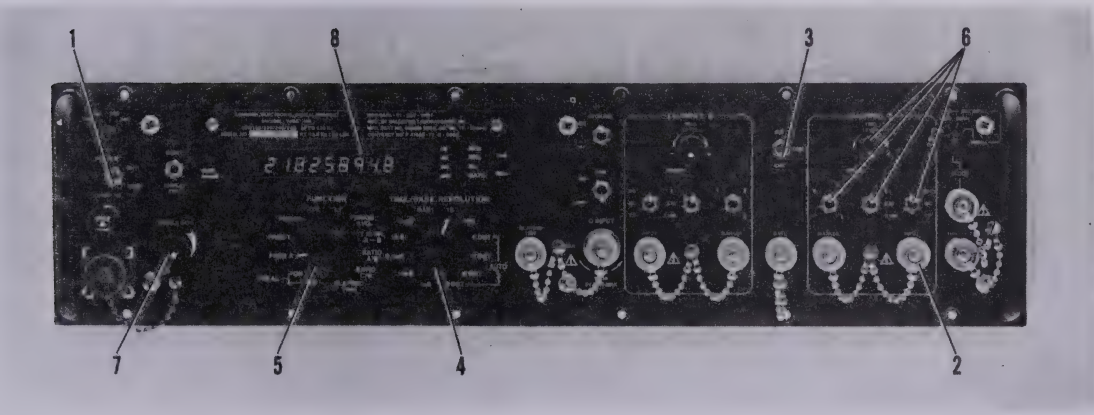

1. Turn POWER switch ON.
2. Connect signal to be measured (0.1 Hz to 110 MHz) to Channel A INPUT connector.
3. Set SEP-COM-CHK switch to SEP.
4. Set TIME BASE/RESOLUTION switch to required time base or desired resolution.
5. Set FUNCTION switch to FREQ A.
6. Adjust Channel A input circuit as outlined in paragraph 3-9.
7. Adjust SAMPLE RATE control for convenient measurement interval.
8. The display reads the frequency of the input signal. The decimal point location and units indicated are dependent on the time base selected. Optimum resolution, units indicated, and correct location of decimal point are automatically computed when in 6, 7, 8, or 9 DGT AUTO position.

Figure 3-3. Operation in FREQ A mode



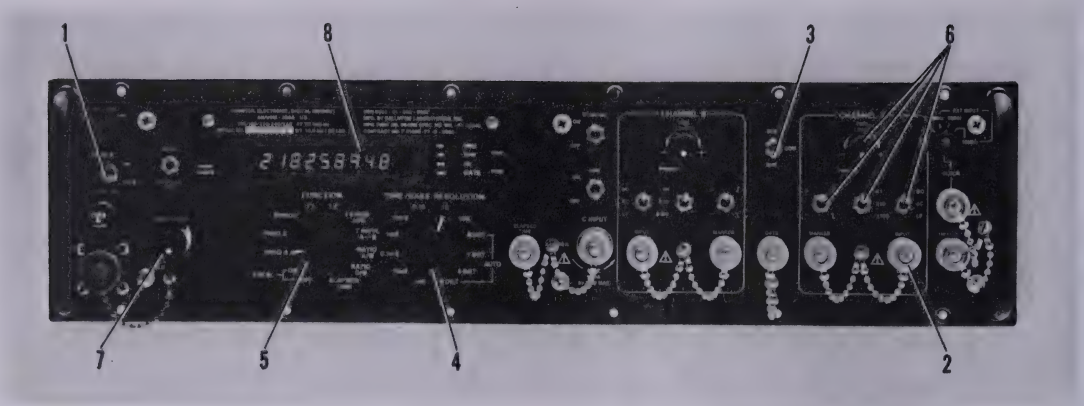

1. Turn POWER switch ON.
2. Connect signal to be measured (30 to 550 MHz) to Channel C INPUT connector. (Be sure signal level does not exceed 5V rms or ±50 Vdc and that signal is from a 50 ohm source or can work into a 50 ohm termination.)
3. Set TIME BASE/RESOLUTION switch to required time base or desired resolution.
4. Set FUNCTION switch to FREQ C.
5. Adjust SAMPLE RATE control for convenient measurement interval.
6. The display reads the frequency of the input signal. The decimal point location and units indicated are dependent on the time base selected. Optimum resolution, units indicated, and correct location of decimal point are automatically computed when in 6, 7, 8, or 9 DGT AUTO position.

Figure 3-4. Operation in FREQ C mode



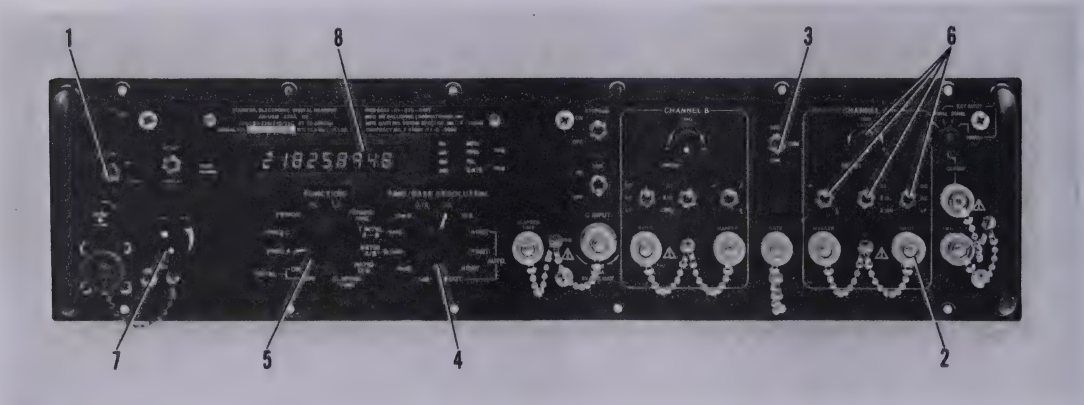

1. Turn POWER switch ON.
2. Connect signal to be measured (100 ns to $10^9$ seconds) to Channel A INPUT connector.
3. Set SEP-COM-CHK switch to SEP.
4. Set TIME BASE/RESOLUTION switch to required time base or desired resolution.
5. Set FUNCTION switch to PERIOD.
6. Adjust Channel A input circuit as outlined in paragraph 3-9.
7. Adjust SAMPLE RATE control for convenient measurement interval.
8. The display reads the period of the input signal. The decimal point location and units indicated are dependent on the time base selected. Optimum resolution, units indicated, and correct location of decimal point are automatically computed when in 6, 7, 8, or 9 DGT AUTO position.

Figure 3-5. Operation in PERIOD mode




1. Turn POWER switch ON.
2. Connect signal to be measured (100 ns to $10^9$ seconds) to Channel A INPUT connector.
3. Set SEP-COM-CHK switch to SEP.
4. Set TIME BASE/RESOLUTION switch to required time base or desired resolution.
5. Set FUNCTION switch to ⎍ Positive or ⎎ Negative Pulsewidth.
6. Adjust Channel A input circuit as outlined in paragraph 3-9.
7. Adjust SAMPLE RATE control for convenient measurement interval.
8. The display reads the width of the positive or negative pulse. The decimal point locations and units indicated are dependent on the time base selected. Optimum resolution, units indicated, and correct location of decimal point are automatically computed when in 6, 7, 8, 9 DGT AUTO position.

Figure 3-6. Operation in ⎍, ⎎ Positive/Negative Pulsewidth modes

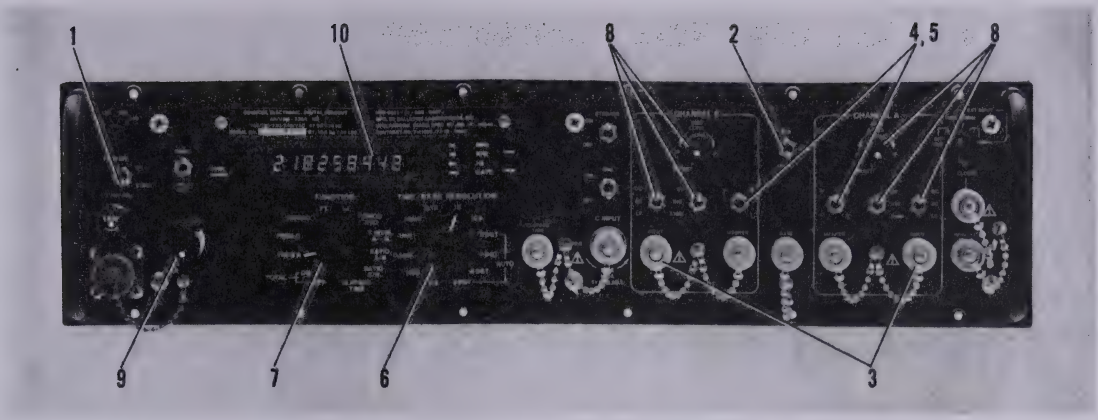



1. Turn POWER switch ON.
2. Connect signal to be measured (0.1 Hz to 10 MHz) to Channel A INPUT connector.
3. Set SEP-COM-CHK switch to SEP.
4. Set TIME BASE/RESOLUTION switch to required time base or desired resolution.
5. Set FUNCTION switch to PERIOD AVG.
6. Adjust Channel A input circuit as outlined in paragraph 3-9.
7. Adjust SAMPLE RATE control for convenient measurement interval.
8. The display reads the average period of the input signal.

NOTE: In this mode, the display range is exceeded if the minimum frequency of the input signal is less than:

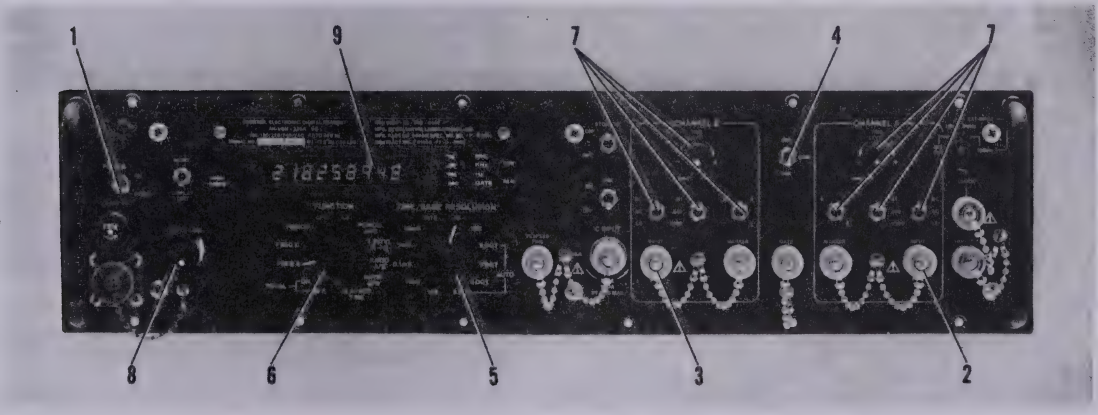
1 Hz with 6-digit resolution
0.1 Hz with 7-digit resolution
0.01 Hz with 8-digit resolution
0.001 Hz with 9-digit resolution

Figure 3-7. Operation in the PERIOD AVG mode



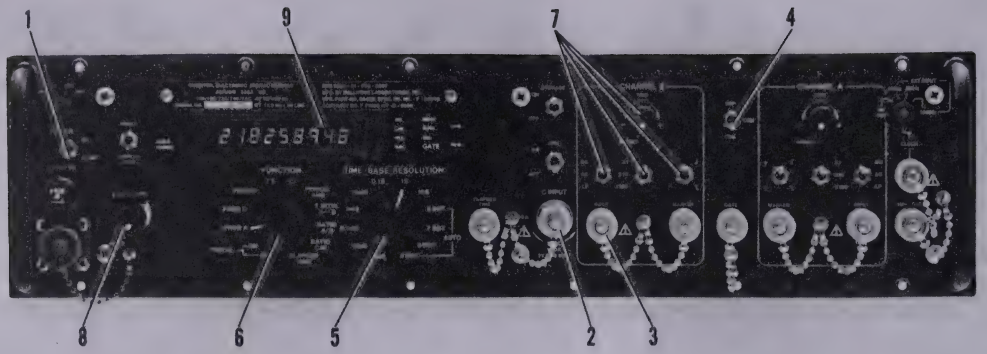

1. Turn POWER switch ON.
2. If separate start and stop signals are to be used, set SEP-COM-CHK switch to SEP. Connect the start signal to Channel A INPUT connector and the stop signal to Channel B INPUT connector.
3. If one signal is to be used to start and stop the count, set SEP-COM-CHK switch to COM. Connect the signal to Channel A INPUT connector.
4. Set Channel A ⌐, ¬ slope switch to start the count on the desired slope.
5. Set Channel B ⌐, ¬ slope switch to stop the count on the desired slope.
6. Set TIME BASE/RESOLUTION switch to required time base or desired resolution.
7. Set FUNCTION switch to T INTVL A→B.
8. Adjust Channel A and Channel B input circuits as outlined in paragraph 3-9.
9. Adjust SAMPLE RATE control for convenient measurement interval.
10. The display reads the time interval between the start signal at Channel A and stop signal at Channel B. Optimum resolution, units indicated, and correct location of decimal point are automatically computed when in 6, 7, 8, or 9 DGT AUTO position.

Figure 3-8. Operation in T INTVL A→B mode



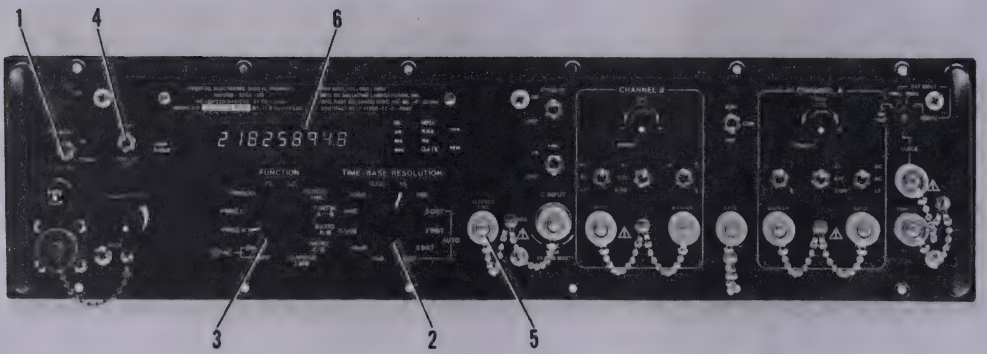

1. Turn POWER switch ON.
2. Connect higher frequency signal to be measured (0.1 Hz to 110 MHz) to Channel A INPUT connector.
3. Connect lower frequency signal to be measured (0.1 Hz to 10 MHz) to Channel B INPUT connector.
4. Set SEP-COM-CHK switch to SEP.
5. Set TIME BASE/RESOLUTION switch to required time base or desired resolution.
6. Set FUNCTION switch to RATIO A/B.
7. Adjust Channel A and Channel B input circuit as outlined in paragraph 3-9.
8. Adjust SAMPLE RATE control for convenient measurement interval.
9. The display indicates the ratio A/NB with an automatically positioned decimal point when in 6, 7, 8, or 9 DGT AUTO position.

Figure 3-9. Operation in RATIO A/B mode




1. Turn POWER switch ON.
2. Connect higher frequency signal to be measured (30 to 550 MHz) to Channel C INPUT connector.
3. Connect lower frequency signal to be measured (0.1 Hz to 10 MHz) to Channel B INPUT connector.
4. Set SEP-COM-CHK switch to SEP.
5. Set TIME BASE/RESOLUTION switch to required time base or desired resolution.
6. Set FUNCTION switch to RATIO C/B.
7. Adjust Channel B input circuit as outlined in paragraph 3-9. Observe 50 ohm input precaution on Channel C.
8. Adjust SAMPLE RATE control for convenient measurement interval.
9. The display indicates the ratio C/NB with an automatically positioned decimal point when in 6, 7, 8, 9 DGT AUTO position.

Figure 3-10. Operation in RATIO C/B mode




1. Turn POWER switch ON.
2. Set TIME BASE RESOLUTION switch to required time base or desired resolution.
3. Set FUNCTION switch to ELAPSED TIME.
4. Return the display to zero by pressing RESET.
5. Short ELAPSED TIME BNC connector to ground to start the timing interval and open the connection to stop the timing interval. This action may be repeated as many times as required. An external switch or saturated transistor to ground may be used to automate or remotely control elapsed time.
6. The display indicates the total elapsed time while the connection of step 5 is made. The units indicated and the correct location of decimal point are automatically computed when in 6, 7, 8, or 9 DGT AUTO position.

Figure 3-11. Operation in ELAPSED TIME mode

# SECTION IV

# THEORY OF OPERATION

## 4-1. INTRODUCTION

4-2. The theory of operation of the AN/USM-326A is discussed in detail in the following paragraphs. This universal counter provides a number of functional capabilities including event counting, measuring both the frequency and period of periodic functions, measuring frequency ratios, pulse width, and time intervals. The instrument provides for both manual and automatic operation. Many of the units serve multiple purposes and in the description that follows each function will be discussed in terms of its major signal paths. Refer to block diagram Figure 4-1 and simplified schematic Figures 6-1 and 6-2.

## 4-3. TOTAL, FREQUENCY AND RATIO FUNCTIONS

4-4-1. In the TOTAL ON, FREQ A and RATIO A/B positions, signals coming through the Channel A amplifier are routed into a gated high speed decade counter on the Channel C Amplifier board, A5. The output is then directed to the display decade counters on the Auto and Display Decades board, A11. The reading of the display counter provides a measure of the number of signal pulses that accumulate between the time the gate is opened and the time it is closed.

4-4-2. In the FREQ C and RATIO C/B positions, the operation is similar except that signals come through the Channel C amplifier and are directed to a separate Channel C gated high speed counter on A5 board.

4-4-3. In TOTAL, the gate is open continuously when switched to the ON position. In FREQ A and FREQ C positions, the gate is opened for a precise period of time determined by the time base multiplier. In positions RATIO A/B and RATIO C/B, the gate is opened for a precise number of signals received through Channel B.

4-4-4. In the circuit descriptions that follow, reference is made to the simplified schematic Figure 6-1 in which the signal paths discussed can be traced.

## 4-5. TOTAL

4-5-1. In the TOTAL ON condition, signals from P7-12 of Channel A Amplifier board, A3 enter the Channel C Amplifier board, A5 at P9-13. The signals are gated through U5 into the "A" high speed decade counter comprised of U6 and U7.

4-5-2. In this condition, the gate control signal from U7-3 on the Function and Logic board, A6 is at a high logic level resulting in a constant "gated-on" condition. After a count of 10, an output signal from the "A" high speed decade counter passes through gate U4 to output P9-2 of A5. The output is connected to the decade counters, U16 through U23 on the Auto and Display Decades board, A11. Transfer of the accumulated count to the display latches U6 through U10 and U12 through U14 is continuous. Signals from the "A" high speed counter on A5 board are routed through multiplexer U8 to the display latch U15 on A11.

## 4-6. FREQUENCY A

4-6-1. In FREQ A, the signals follow the same path as in TOTAL ON. However, the gate control signal from U7-3 of A6 restricts the flow of signals that pass through the "A" high speed counter to a preselected period of time. The sequence of events that control the turning on and off of the gate will be described in the following paragraphs.

4-6-2. The 10 MHz clock signal from P4-4 of the Time Base and Clock Control board, A1 is directed through gate U5 on the Chain Divider board, A7 to decade counter U7. The 1 MHz output signal from U7 passes through gate U4 to P3-5 on A7 board. From there, the 1 MHz signal interconnects to gate U3 "START" on board A6. The low-to-high transition from U3 to U5 through C2 results in a low signal at U5-3 and a high transition at the clock input terminal U6-11. This causes the $\overline{Q}$ output at U6-8 to go low and the gate control signal at U7-3 to go high, activating the high speed counter U6 on board A5. At the same time, U6-6 on board A6 is flipped to low level preparing the gate to be turned off by the next clock input transition to U6.

4-6-3. The output from U4 on the Chain Dividers board, A7 is also directed to flip-flop U1 on the Function and Logic board, A6. This flips U1-8 low and U2-6 high and in turn U4-12 is low and U4-8 is high. While the signal is being gated, U6-9 is at a high level causing U4-6 to be low. U5-3 goes high and U5-6 goes low preparing the gate to be turned off at the start of the next high signal.

4-6-4. The gate signal from U7-3 on A6 also enables gate U7 on the Reset and Arming board, A8. This gates the 1 MHz signals from U4, A7 to the decade counters U9 through U15 on A7. After a number of counts determined by the resolution control signals into multiplexer, U16, an output pulse from U16-15 is directed to P3-15 on A7. This pulse is interconnected to P10-24 on the Function and Logic board, A6. It is coupled through C1 to U1 causing a momentary high at the output of U1 and results in U4-6 going high.

4-6-5. The next 1 MHz clock pulse from U4-8 on A7 is directed to U3 on board A6. It couples through C2

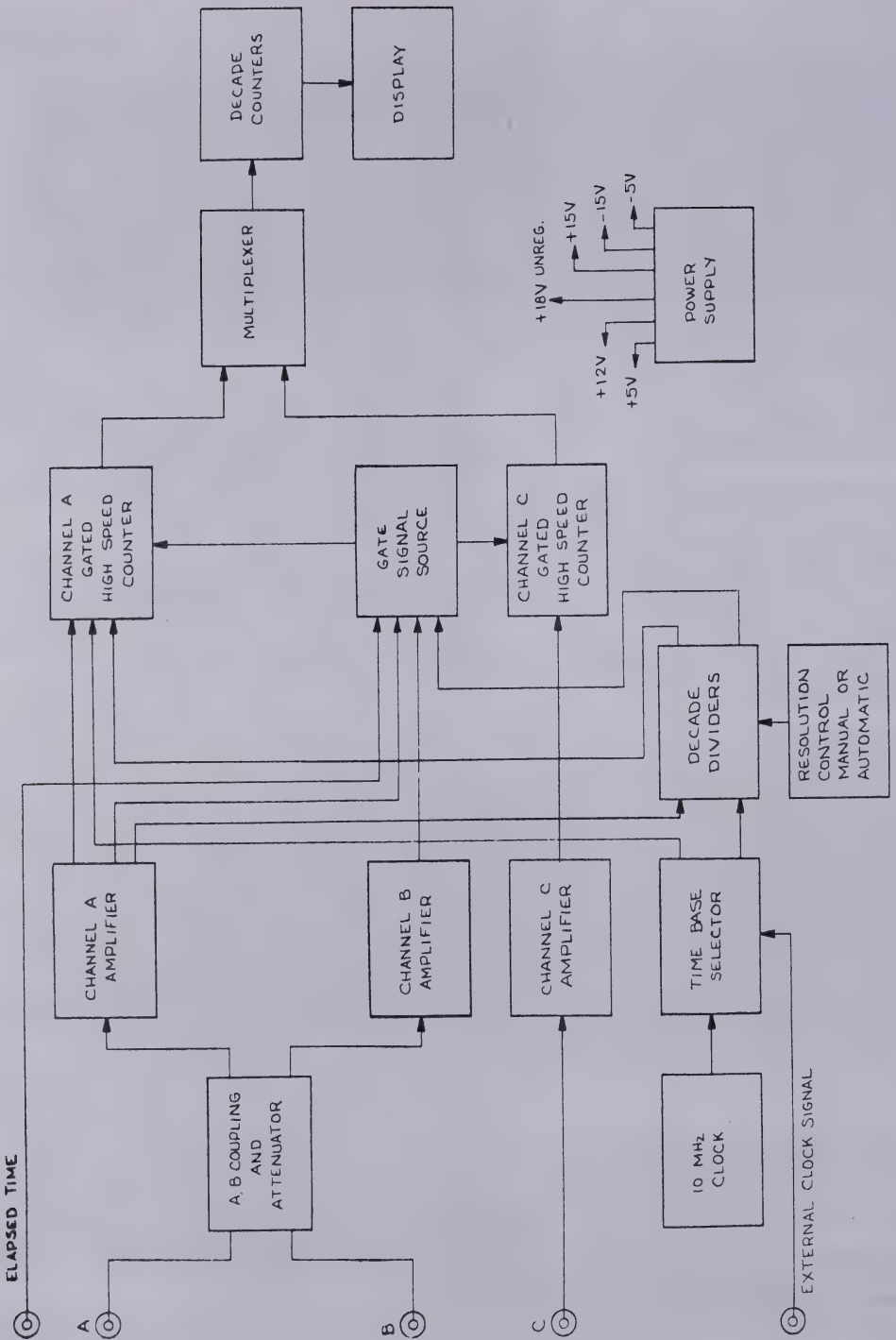



Figure 4-1. Functional Block Diagram

to U5 causing U6 to turn off the gate. Since flip-flop U6 is at a low level, the gate cannot be turned on again until the circuit is reset by a signal which flips U6-6 high, U6-8 high, U6-9 low and U4-8 high. This resets the "A" high speed decade counter on A5, decade counters U16 through U23 on A11, as well as the decade counters U9 through U16 on A7 to zero.

4-7. FREQUENCY C

4-7-1. Operation in FREQ C is similar to that of FREQ A. The signal to be measured is applied directly to the Channel C amplifier U1 on board A5. The signal is then coupled to the "C" high speed decade counter U2.

4-7-2. A logic "high" DC signal is applied to U4-2 on A5 through P9-3 in the FREQ C position. This enables gate U4 permitting the flow of signals from the output of the "C" high speed decade counter into the decade counters, U16 through U23 on A11. This same DC signal biases transistor Q1 on A5 "on" causing a low level signal at U4-13. This shuts off the flow of signals from the "A" high speed decade counter U6 and U7. The DC signal also is applied to control pin 1 of the multiplexer, U8, directing the BCD output of counter U2 to display latch U15 on A11.

4-7-3. In the FREQ C mode, the gate control signal from U7-3 on board A6 is directed to the TTL/ECL converter, U3 on A5. This provides gating control for the flow of signals in "C" high speed decade counter U2.

4-8. RATIO A/B

4-8-1. Signal flow in this position of the FUNCTION switch is similar to that of FREQ A except that the gate is controlled by input signals through Channel B amplifier, A4, instead of the 10 MHz clock signal.

4-8-2. Signals from the output of the Channel B amplifier are connected from P8-12 on board A4 to P3-11 on the Chain Divider board and then directed to U3-2. The signal is gated through either U3-3 or U3-8 depending on the position of the slope switch. From U3-11, the Channel B signal passes through gate U4 on A7. At this point, the operation of the gate control circuitry is identical to that described in 4-6.

4-9. RATIO C/B

4-9-1. In this position of the function switch, the flow of signals is from Channel C to the decade counters as described in 4-7, instead of from Channel A.

4-9-2. The flow of gate signals is through Channel B. The circuit description is exactly as that discussed in 4-8.

4-10. PERIOD, PULSEWIDTH, TIME INTVL AND ELAPSED TIME

4-11. Each of the six time functions use a clock signal path and a gate control path. These will be described in the sections that follow.

4-12. PERIOD

4-12-1. In this mode, a single period of a signal from Channel A turns on and then off, the gate controlling the flow of timing signals.

4-12-2. The 10 MHz clock signals from the Time Base Mult and Clock Control board, A1 is interconnected to gate U5 and then to gate U4 on the Chain Dividers board, A7. It is then directed to gate U7 on the Reset and Arming board, A8, and next back to board A7 where it is applied to decade counters U9 to U15. From the decade counters, the signal is applied to multiplexer U16 which is controlled by the setting of the Time Base/Resolution switch.

4-12-3. The multiplexed signal is first gated through U2 on board A6 and then through U5 on A5. From there it goes into a binary-coded decimal counter comprised of flip-flops U6 and U7. The output then interconnects to the display counters U16 through U23 on board A11.

4-12-4. The sequence may be summarized as follows. A reset signal sets all of the decimal counters to zero. The 10 MHz clock signal is then gated on and off by Channel A signal leaving a number in the decade counters which indicates the time elapsed during one cycle of the "A" signal. This count is then transferred into the display latches U7 through U15 on A11.

4-13. PULSEWIDTH

4-13-1. Pulsewidth measurements utilize the midpoints of opposite slopes of a signal applied at Channel A to open and close the gate. Aside from that, the circuits operate precisely as described in PERIOD mode. Positive pulsewidth measurements are identified by the symbol ⎍ and negative by ⎏.

4-13-2. The signals from Channel A amplifier pass through inverter U5-3 on board A5 to board A7 where the start and stop pulses are separated and from there follow parallel channels. The positive start pulse passes through inverters U5-8 and U2-8 on the Reset and Arming board, A7 and then through inverter U3-8 on A6. It is coupled through C2 to U5-3 and U5-6 where it turns on the control gate, U7. The positive stop pulse passes through gate U2-6 on A7 to gate U3-6 on A6. It is coupled through C3 to gates U5-11 and U5-6 to turn off the control gate, U7. A low control signal from A6-5 and a high from A6-6 accomplish the routing of these two signals.

4-13-3. The negative start pulse passes through inverter U2-8 on A7 and then through inverter U3-8 on A6 to turn on the control gate. The negative stop pulse passes through inverters U5-8 and U2-6 on A7 and then to inverting gate U3-6 on A6 to turn off the control gate. A high control signal from A6-5 and a low one from A6-6 accomplish this routing of the two signals.

4-14. TIME INTERVAL A→B

4-14-1. In this mode, the gate is turned on by a signal from Channel A and turned off by a signal from Channel B. Each of these signals may operate on either a positive or negative slope as selected by the Channel A and B ⎍, ⎏ switches. The clock signal path is the same as that described in 4-12-2.

4-14-2. The Channel A signal that turns on the gate passes through inverter U5-3 on board A5 and then interconnects to board A7. Here, the signal may follow either of two paths depending on the setting of Channel A ⎍, ⎏ slope control. On the positive (⎍) slope, the signal passes through U2-1 to U2-8. On the negative (⎏) slope, it passes through inverter U5-8 on A7 and then through U2-10 to U2-8. From U2-8, the start signal passes through gates U3-10 and U3-8 on A6. The signal is coupled through C2 to gates U5-3 and U5-6 to turn the gate control flip-flop U6 on. When the gate turns on, U6-8 on A6 goes low and gate U5-8 on board A5 turns "A" high speed decade counters on. Gate U7-8 on the Reset and Arming board, A8 is also turned on. U6-9 going high opens gate U5-11 to stop the signals. U4-6 goes low, closing gate U5-3 until a reset signal is received.

4-14-3. The stop signal interconnects from Channel B amplifier on A4 to board A7. Here, it passes either through inverters U3-6 and U3-8 or only through inverter U3-3, depending on the setting of Channel B ⎍, ⎏ slope control. In either case the turn-off signal is a high to low transition at U3-11 on A7. The stop pulse then passes through U3-5 and U3-6 on A6, is coupled through C3 to U5-11 and U5-6 to turn off the gate control flip-flop U6. The gate remains off until a reset signal is received at U6-1 on A6.

4-15. PERIOD AVERAGE

4-15-1. In this position, the timing signals from the 10 MHz clock pass through a decade counter before being gated. The gating is now controlled by a selected decimal multiple of Channel A signals so that the period measurement represents an average of the periods of many sequential signals. This function is particularly useful in averaging out reading errors caused by the presence of "white noise."

4-15-2. The 10 MHz clock signal passes through gate U5-11 on A7 and into decade counter U7 to produce a 1 MHz timing signal. This signal passes through gates U2-11 and U2-8 in A6. From here it goes to inverter U5-6 and gate U5-8 on A5 to the "A" high speed decade counter U6 and U7. The output is then interconnected to the decade counters U16 through U23 on board A11. In this condition the counters are gated on by a high level logic signal at U6-2 and 3 on A5 and gated off by a low level signal.

4-15-3. The routing of the gating signal for the PERIOD AVG function starts from the Channel A amplifier, A3. It interconnects to inverter U5-3 on A5 and then to the input P3-12 on board A7. Here it may take either of two paths to gate U2-8 depending on the position of Channel A ⎍, ⎏ slope switch. From U2-8 it passes through gate U4-8.

4-15-4. The signal from U4-8 passes through gate U3-8 on A6 and is coupled through C2 to gates U5-3 and U5-6. It then gates on flip-flop U6-9 as well as flip-flop U1-8. This puts a low signal at the input of gate U2-6. As the gate turns on, U7-3 on A6 goes high, opening gate U7-8 on the Reset and Arming board, A8, to the Channel A signals from U4-8 in A7. These signals are then directed to the decade counters U9 through U15 on the Chain Dividers board, A7.

4-15-5. After a preselected number of counts, determined by the resolution control logic to multiplexer U16 on A7, the output of U16 goes low and resets flip-flop U8-1 on A6 to a high level. The output of gate U2-6 then goes low, flipping U4-8 low and putting a high signal on gate U4. The next high-to-low transition of Channel A signal from U4-8 on A7 is inverted in gate U3-8 providing a turn-off signal for flip-flop U6-9 on A6. As the gate control signal from U7-3 on A6 goes low, the count at U6 on board A5 is stopped. The counters on A5 and A11 then hold the count until it is transferred into the display latches U6 through U15 on A11 by a transfer signal.

4-16. ELAPSED TIME

4-16-1. In ELAPSED TIME mode the gating period is controlled by an external contact closure to ground at the ELAPSED TIME BNC connector. The clock signal path is identical to that described in PERIOD mode.

4-16-2. The gating signal is applied at the front panel ELAPSED TIME connector. This closure to ground puts a low level signal at gate U7-13 on board A6 and results in a high signal at U7-3. This opens gate U7-8 on A8 and enables decade counter U6 on A5. At the end of the gating period, the count is held in counters U6 and U7 on A5 and U16 through U23 on board A11 until a reset signal is received.

4-17. SAMPLE RATE AND RESET

4-17-1. At the end of a measurement, the count in the display counters is transferred into the display latches. The operator can adjust the amount of display time by means of the SAMPLE RATE control on the front panel. When the control is set to HOLD, the display is held indefinitely until the RESET button is depressed.

4-17-2. For operation of this circuit refer to Figure 4-2. Current supplied by +15V flows through the SAMPLE RATE potentiometer R26 into capacitor C5 on the Reset and Arming board, A8. When the voltage reaches a certain level, unijunction transistor Q1 conducts and discharges C5. This rate is determined by the setting of R26. When Q1 conducts, a momentary low signal is coupled through C4 to U1. This puts a momentary high at C6 causing Q3 to conduct.

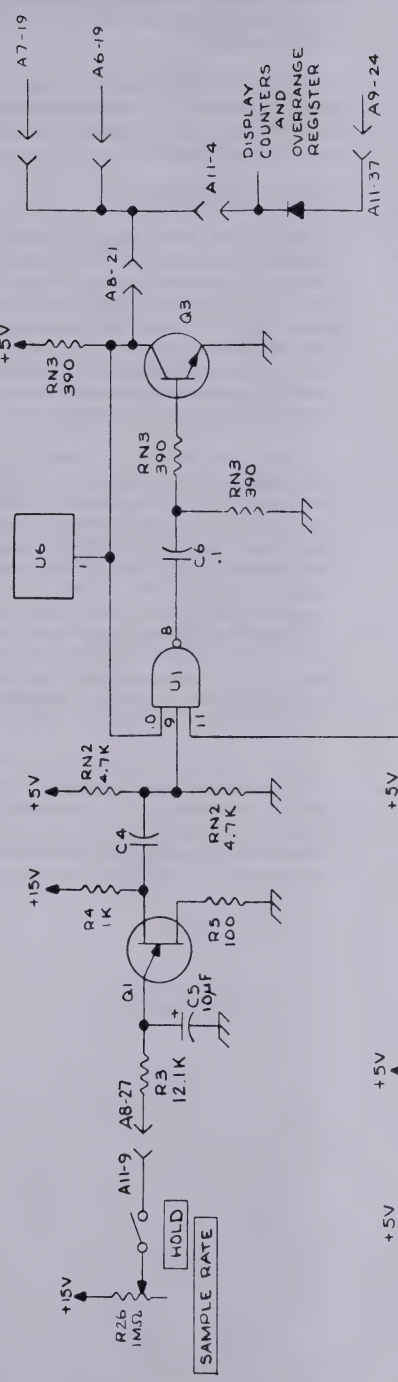



Figure 4-2. Simplified Schematic, Sample Rate and Reset

As Q3 conducts, U1-10 goes low, generating a sharp negative reset signal. Its duration is about 20 us, determined by C6 and RN3. The SAMPLE RATE permits a display time from less than 200 ms to more than 5 seconds.

4-17-3. When the SAMPLE RATE control is set to the detented HOLD position, switch S3 opens and the display is held until the manual RESET pushbutton is depressed. This puts a momentary low at U26-13 on board, A11; a momentary high at U39-6 and a momentary low at U1-11 on A8. This generates a reset signal which is applied to the collector of Q3.

4-17-4. The reset signal initializes a number of individual units in the counter. The Channel B sync register U6-6 on board A8 and the gate control flip-flops U1, U4-8, and U6 on A6 are reset. On A7, the counters U7 and U9-15 are reset. The "C" high speed counter, U2 and the "A" high speed counter, U6 and U7 on A5 are reset as well as U10, the synchronization flip-flop. On the Auto and Display Decades board, A11; the display counters U16 through U23 and the automatic programing counter U37 are reset. Diode C13 resets the over-range register U30-5.

## 4-18. SYNCHRONIZATION AND ARMING

4-18-1. In FREQ A and FREQ C modes the operator is given a choice of continuous readings (ARM OFF) or of waiting for a trigger signal through Channel B (ARM ON). Refer to simplified schematic Figure 4-3.

4-18-2. In the ARM OFF position, Channel A or C input signals turn on flip-flop U10-6 or U10-8 on board A5 so that a high-to-low transition at U11-6 is synchronous with the signal. U5-11 on board A8 is high. U5-6 is low and U5-3 is high. The turn-on signal makes U3-6 high, U3-8 low and U5-3 high on board A7. This gates on the flow of signals from the 10 MHz clock.

4-18-3. When ARM is ON, U5-11 on board A8 is low and U5-6 is high. The turn-on of flip-flop U6-6 on A5 by signals from Channel B enables gates U3-11 and U3-8 on board A8.

## 4-19. POWER SUPPLY

4-19-1. The power supply for the AN/USM-326A is contained on board A2. AC power at a frequency of 50 to 400 Hz and at any one of four voltages; 100V AC, 120V AC, 220V AC, 240V AC is applied through switch S3. It enters the instrument through a three pin panel connector, A15 J1 and a line filter FL1. Two power transformers are used, each individually fused. T1 supplies power to the main power supply while T2 powers the crystal oven.

4-19-2. One secondary winding of transformer T1 is rectified by CR4 and CR5. This rectified voltage is filtered by C10 to provide +9 Volts DC which is directed to individual +5 Volt regulators on circuit boards A1 and A11. Another secondary is rectified by diodes CR6 and CR7. This voltage is filtered and applied to regulators U4 and U5. These also provide regulated voltages of +5V. Still another secondary of T1 is rectified by the bridge CR3. This filtered voltage is directed to U1 and U6 to provide -5V DC and -15V DC respectively. The same filtered voltage is applied to U7 to supply a regulated voltage of +15V DC and to U3 to supply a regulated voltage of +12V DC.

4-19-3. The secondary of T2 is rectified by diodes CR1 and CR2. This voltage is filtered and then applied to regulator U2. The output of this regulator, +12V DC, is directed to the crystal oscillator, Y1. Power is applied to the primary of T2 as long as the power cable is connected to a mains.

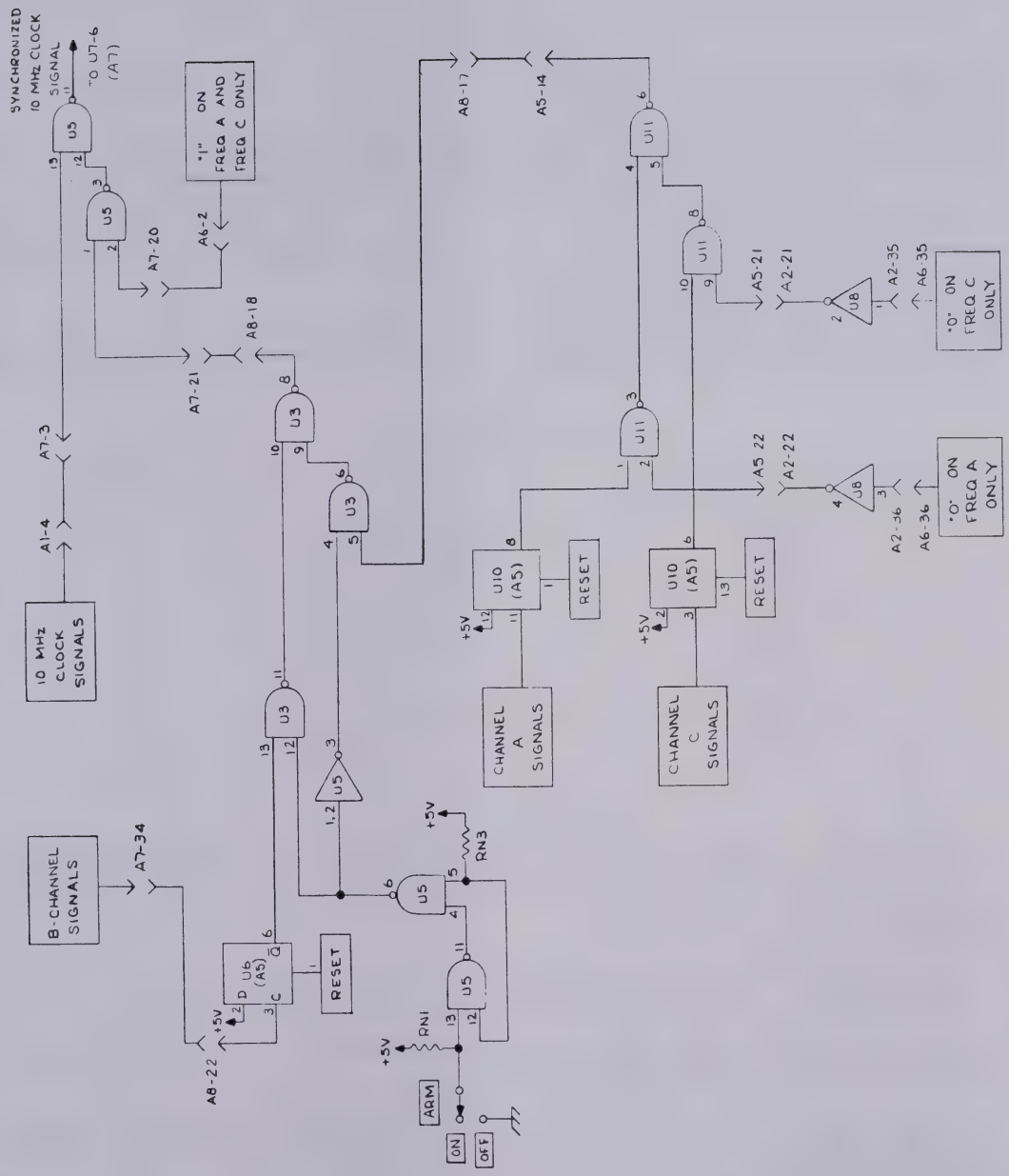



Figure 4-3. Simplified Schematic, Synchronization and Arming

# SECTION V

# MAINTENANCE

## 5-1. INTRODUCTION

5-2. This section contains information required for maintenance of Universal Counter AN/USM-326A. Included are a table of assemblies (Table 5-1), table of recommended test equipment (Table 5-2), calibration and adjustment procedures, and an in-cabinet performance check. Refer to paragraph 5-20-1 for instructions on removal of the instrument from its case.

5-3. The data provided is within the capabilities using common tools, test equipment and spare parts authorized in allowance lists.

5-4. Although the AN/USM-326A is ruggedly built, it contains precision components. To prevent damage, handle the instrument carefully. If possible, repair in a well ventilated, dust-free room to prevent contamination from dust, grease, moisture, metal chips, or other foreign matter.

## 5-5. SPECIAL TOOLS AND TEST EQUIPMENT

5-6. The only special tool required for maintenance of the AN/USM-326A Counter-Timer is a JFD Alignment Tool, No. 5284 or equivalent. The test equipment required to check, calibrate, and maintain the AN/USM-326A is listed in Table 5-2. Equivalent test equipment may be substituted if the recommended test equipment is not available.

Table 5-1. Assembly Identification

| ASSEMBLY | DESCRIPTION | BALLANTINE PART NO. |
|---|---|---|
| A1 | Time Base and Clock Control | 89-10623-1A |
| A2 | Power Supply and Interconnect | 89-10622-1A |
| A3 | Channel A Amplifier | 89-10579-1A |
| A4 | Channel B Amplifier | 89-10582-1A |
| A5 | Channel C Amplifier | 89-10587-1A |
| A6 | Function and Logic | 89-10589-1A |
| A7 | Chain Dividers | 89-10604-1A |
| A8 | Reset and Arming | 89-10601-1A |
| A9 | Attenuator | 89-10578-1A |
| A11 | Auto and Display Decades | 89-10624-1A |
| A12 | Display | 89-10607-1A |
| A15 | Front Panel | 89-10803-1A |

Table 5-2. Test Equipment

| EQUIPMENT NUMBER | NOMENCLATURE | USE AND APPLICATION | REQUIREMENT |
|---|---|---|---|
| TEKTRONIX TYPE 191 | Signal Generator | DC Balance Adjustment. | 50 kHz to 100 MHz, 5 mV to 5V constant amplitude sinewave generator. |
| BALLANTINE 1040A | Oscilloscope | Performance Testing and general troubleshooting. | Dual Trace, DC to 40 MHz bandwidth. |
| BALLANTINE MODEL 3028B | Digital Multimeter | Performance Testing, Calibration and general troubleshooting. | Measure AC/DC voltages from 20 mV to 200V. |
| BALLANTINE MODEL 6130A | Time Mark Generator | Oscillator Calibration. | Multiply 10 MHz frequency standard 50 X, providing a 500 MHz sinewave. |
| HEWLETT PACKARD MODEL 3200B | VHF Oscillator | Supply reference signals for performance testing. | 10 MHz to 500 MHz. |

Table 5-2. Test Equipment (Cont)

| EQUIPMENT NUMBER | NOMENCLATURE | USE AND APPLICATION | REQUIREMENT |
|---|---|---|---|
| BALLANTINE MODEL 5500B | Counter-Timer | Measure sample rate. | dc-110 MHz frequency range. |
| HEWLETT PACKARD MODEL 105A/B | Frequency Standard | Supply reference signal for oscillator stability checks. | 1 MHz Frequency Standard. |
| HEWLETT PACKARD MODEL 651B | Test Oscillator | Supply reference signals for performance testing. | 10 Hz to 10 MHz sinewave. |

## 5-7. PERFORMANCE ASSURANCE TEST

5-8. The performance checks outlined in Section 3-6 verify the operation of most circuits in the AN/USM-326A and may be used for any of the following:

a. As part of an incoming inspection check of instrument performance.

b. Periodically, for instruments used in systems.

c. As part of a troubleshooting procedure.

d. After any repairs or adjustments, before returning the instrument to service.

5-9. The following are more extensive operational tests that when performed in addition to the checks of 3-6 verify proper functioning of all circuits in the AN/USM-326A. They should be conducted periodically to insure that a satisfactory performance level is maintained.

### 5-9-1. INTERNAL OSCILLATOR TIME BASE STABILITY

a. Set the front panel controls as follows:

| | |
|---|---|
| SAMPLE RATE | FULL CW |
| FUNCTION | FREQ A |
| TIME BASE/RESOLUTION | 10S |
| ⌐, ⌙ (Slope, Channel A) | + |
| DC/AC/LF (Channel A) | DC |
| X1/X10/X100 (Channel A) | X1 |
| TRIG LEVEL (Channel A) | PRESET |
| SEP-COM-CHK | SEP |
| STORAGE | ON |
| CLOCK | INT OUT |
| ARM | OFF |

NOTE

Allow a 30 minute warm-up before proceeding to step b.

b. Connect 1 MHz frequency standard to INPUT A.

c. A counter display of 1000000.0 Hz indicates that the internal time base oscillator frequency is exactly 10 MHz. Any offset between AN/USM-326A time base and the 1 MHz frequency standard is determined by subtracting 10 MHz from 10 X counter display reading. A negative offset means that the internal time base is higher by that amount. A positive offset means it is lower by that amount.

| Counter Display X 10 | Offset (Minus 10 MHz) | Internal Time Base |
|---|---|---|
| 9999980 Hz | -20 Hz | 10000020 Hz |
| 1000000 Hz | 0 | 10000000 Hz |
| 10000020 Hz | +20 Hz | 9999980 Hz |

d. Record the frequency offset. For long term stability measurement, operate the AN/USM-326A continuously for at least one week. Measure the frequency offset at one month intervals.

e. To calibrate the counter time base to the frequency standard, perform time base adjustment described in paragraph 5-21.

### 5-9-2. INTERNAL OSCILLATOR TIME BASE OUTPUT

a. Set front panel controls as outlined in 5-9-1a.

b. Connect 1040A Oscilloscope CH1 vertical input to 1 MHz BNC connector.

c. Oscilloscope should display 1 MHz sine wave at $\approx$ 1 Volt peak to peak.

d. Connect the oscilloscope vertical input directly to the CLOCK BNC connector.

e. Oscilloscope should display 10 MHz squarewave with amplitude $\geq$ 3 Volt peak to peak.

f. Disconnect all test equipment from the counter.

### 5-9-3. FREQUENCY RESPONSE AND SENSITIVITY

a. Set front panel controls as outlined in 5-9-1a, except RESOLUTION to 1s and DC/AC/LF (A) to AC.

b. Connect a BNCT connector to INPUT A. Connect 651B Test Oscillator 50 Ω output to T connector. Connect oscilloscope CH1 vertical input to T connector to monitor input signal amplitude; use a 50 Ω feedthrough at oscilloscope BNC.

c. Adjust test oscillator from 10 Hz to 10 MHz maintaining 80 mV rms (226 mV p—p) input amplitude. Counter should properly display all frequencies within this range.

d. Disconnect 651B Test Oscillator and connect 3200B VHF Oscillator to T connector.

e. Adjust test oscillator from 10 MHz to 100 MHz maintaining 80 mV rms (226 mV p—p) input amplitude. Counter should properly display all frequencies within this range.

f. Disconnect 3200B and re-connect 651B to T connector.

Channel C sensitivity check; using channel C specification on page 1-5, frequency C mode is same as frequency A mode except the signal input is connected to channel C.

g. Adjust 651B Test Oscillator output to 1000 Hz at 5 volts peak-to-peak.

h. Connect Channel A MARKER of AN/USM-326A to CH2 of oscilloscope.

i. Set SEP-Com-CHK to COM.

j. Set the oscilloscope to alternate sweep with internal triggering from oscilloscope CH1. Select sweep speed of lms/cm.

k. Adjust oscilloscope for a symmetrical waveform on CH1, centered at 0 volts. Adjust CH2 trace position so that top of Channel A marker pulse is at 0 volts. (The top of marker pulse A should touch both the positive and negative slope of the waveform. This indicates that the trigger level is at 0 volts in the PRESET position.)

l. Adjust CH2 trace position so the top of the marker pulse is 2.5 volts above 0 volts. Rotate Channel A TRIG LEVEL control until the top of the marker pulse touches both the positive and negative slope of the waveform. This indicates that the trigger level is at 2.5 volts.

m. Rotate Channel A TRIG LEVEL control from full CW position to CCW. Top of marker pulse should be settable to at least 2.5 volts below 0 volts.

n. Disconnect cable from Channel A MARKER of AN/USM-326A and connect it to Channel B MARKER. Repeat steps k through m.

o. Disconnect all test equipment from the counter.

5-9-4. PERIOD, PERIOD AVG, POSITIVE AND NEGATIVE PULSEWIDTH

a. Set front panel controls as outlined in 5-9-1a, except FUNCTION to PERIOD.

b. Connect a BNCT connector to INPUT A. Connect 651B Test Oscillator 50 Ω output to T connector. Connect 1040A Oscilloscope CH1 vertical input to T, using 50 Ω feed-through at oscilloscope BNC.

c. Vary the test oscillator from 10 Hz to 10 MHz, maintaining 80 mV rms amplitude. Switch TIME BASE/RESOLUTION as needed to maintain meaningful display with change of frequency. Counter should properly display the period of the frequencies in this range.

d. Rotate FUNCTION switch to PERIOD AVG and repeat step c. Counter should properly display the period average of the frequencies in this range.

e. Rotate FUNCTION switch to ⎍ (Positive Pulsewidth) and repeat step c. Counter should properly display the pulsewidth of the frequencies in this range. Note that the display is approximately half that observed in step c for any given frequency.

f. Rotate FUNCTION switch to ⎎ (Negative Pulsewidth) and repeat step c. Counter should properly display the pulsewidth of the frequencies in this range. Note that the display is approximately half that observed in step c for any given frequency.

5-9-5. TIME INTERVAL

a. Set the front panel controls as follows:

| | |
|---|---|
| SAMPLE RATE | Midrange |
| FUNCTION | T INTVL A→B |
| TIME BASE/RESOLUTION | 1 us |
| (Slope, Channel A) | + |
| (Slope, Channel B) | - |
| DC/AC/LF (Channel A and B) | AC |
| X1/X10/X100 (Channel A and B) | X1 |
| TRIG LEVEL (Channel A and B) | PRESET |
| SEP-COM-CHK | COM |

b. Connect 651B Test Oscillator to INPUT A. Set oscillator frequency to 1 MHz and adjust output level for 150 mV rms (424 mV p-p).

c. Display should indicate 0.5 us ± 1 count trigger error.

5-9-6. TOTALIZE

a. Connect 651B Test Oscillator to INPUT A. Set oscillator frequency to 1 MHz and adjust output level for 80 mV rms (226 mV p-p).

b. Set front panel controls as outlined in 5-9-5a except FUNCTION to TOTAL OFF, TIME BASE/RESOLUTION to 1s and SEP-COM-CHK to SEP.

c. Check that GATE annunciator light is out and display indicates zero after RESET button is actuated.

d. Switch FUNCTION to the TOTAL ON position and observe that GATE light is on and that display counts.

e. Set FUNCTION switch back to TOTAL OFF. Note that GATE light is out and that accumulated count is displayed.

f. Repeat steps d and e. Observe that count continues to totalize.

g. Depress RESET and note that the display returns to zero after the button is released.

5-9-7. ELAPSED TIME

a. Rotate the FUNCTION switch to ELAPSED TIME, the TIME BASE/RESOLUTION to 1s and turn the SAMPLE RATE control full CW.

b. Zero the count by momentarily depressing RESET. Check that the GATE light is out.

c. Ground the center pin of the ELAPSED TIME BNC connector and observe that a count is initiated and that the instrument continues to count for as long as the input to the ELAPSED TIME BNC remains grounded. Also note that the GATE light is on.

d. Disconnect the ground. Observe that the display is held and the GATE lamp again extinguishes.

5-9-8. RATIO A/B AND C/B

a. Set counter controls as follows:

| | |
|---|---|
| FUNCTION | RATIO A/B |
| TIME BASE/RESOLUTION | 10 ms |
| ⌐, ¬ (Slope, Channel A and B) | + |
| DC/AC/LF (Channel A and B) | AC |
| X1/X10/X100 (Channel A and B) | X1 |
| SEP-COM-CHK | COM |

b. Connect 651B Test Oscillator to INPUT A. Set oscillator frequency to 10 MHz and adjust output level for 80 mv rms (226 mv p-p).

c. Display should read 1.0000 ±1 count.

d. Connect 3200B VHF Oscillator to C INPUT. Set oscillator frequency to 50 MHz and adjust output level for 50 mV rms (141 mV p-p).

e. Set FUNCTION switch to RATIO C/B.

f. Display should read 5.0000 depending on accuracy of test oscillator setting.

5-9-9. GATE OUTPUT AND SAMPLE RATE

a. Connect the GATE output of the AN/USM-326A to Channel A input of Model 5500B Counter-Timer. Adjust the 5500B by setting FUNCTION to⌐¬, RESOLUTION to 6, SLOPE to⌐, ATTEN to X10, and position the TRIG LEVEL slightly clockwise from center position.

b. Rotate the AN/USM-326A SAMPLE RATE control fully CW and observe that the reading on the 5500B counter is $< 200$ ms.

c. Turn the AN/USM-326A SAMPLE RATE control counterclockwise until just before the HOLD detent. Check that the reading on the 5500B counter is $> 5$ seconds.

d. Disconnect all test equipment.

5-10. INSPECTION AND PREVENTATIVE MAINTENANCE

5-11. An inspection and preventative maintenance check chart is given in Table 5-3. Inspection should be performed on a regular schedule. Where the AN/USM-326A Counter-Timer is not subjected to severe or unusual operating conditions, the recommended time period is six months. In addition to Table 5-3, check the following:

a. That the exterior of the case and protective cover do not shown signs of damage or abuse.

b. That the two hinges and latches that fasten the protective cover to the cabinet are not damaged.

c. That the control panel is undamaged, the hardware is secure, and that the controls operate freely.

d. That all BNC connector covers are attached and that they can be connected and disconnected freely.

e. That the control panel connectors do not have bent, loose, or corroded pins.

f. That all of the required accessory equipment is available in the storage compartment of the protective front panel cover.

Table 5-3. Inspection Requirements

| INSPECT | CHECK FOR | REMEDIAL ACTION |
|---|---|---|
| Chassis | Dents, scratches, deformation, corrosion, damaged hardware. | Straighten, touch up paint, remove corrosion, replace damaged hardware. |
| Connectors | Broken sheels, cracked insulation, deformed contacts, corrosion, faulty solder. | Replace shells, insulation, and contacts; remove corrosion, resolder as necessary. |
| Resistors | Cracked, broken, blistered or charred bodies; poor connections. | Replace faulty resistors, resolder as necessary. |
| Capacitors | Case damage. Loose, broken, or corroded terminal studs, lugs, or leads. Poor solder. | Replace capacitor if case is damaged. Remove corrosion, resolder solder joints. |

Table 5-3. Inspection Requirements (Cont)

| INSPECT | CHECK FOR | REMEDIAL ACTION |
|---|---|---|
| Semiconductors | Mechanical damage. Loose, broken, poorly soldered or corroded terminals. | Replace or repair. Clean and resolder terminals where indicated. |
| Transformers | Overheating; case damage, poor terminal connections, damaged hardware. | Replace defective transformers, resolder terminals as required, replace damaged or missing hardware. |
| Printed Circuit Boards | Loose, broken, corroded, or poorly soldered terminal connections. Inspect for any evidence of damage; such as burned, broken, cracked, or corroded plating. Inspect for loose mounting. | Resolder terminals, repair cracks or other damage. Tighten loose mountings. |
| Soldered Connections | Cold solder or rosin joints, as indicated by rough, dull appearance; excess solder, solder particles adhering to insulation and components. | Resolder faulty connections, remove excess solder and traces of corrosion. |
| Wiring | Charring and physical damage, lead dress in relation to chassis and wiring. | Replace damaged wires, insulate bare wires that may contact chassis or other metal parts. |
| Covers | Dents, scratches, corrosion, damaged fasteners. | Straighten, touch-up paint, remove corrosion, replace damaged fasteners. |
| Gaskets | Tears, creases, folds, rough surface, elongation. | Replace damaged gaskets. |

## 5-12. TROUBLESHOOTING

WARNING

With the AN/USM-326A removed from its case and primary power applied, hazardous voltages are exposed which can cause personal injury. Observe all safety precautions.

5-13. The troubleshooting procedures should only be performed when the instrument fails to meet its specified performance assurance tests. Should the instrument be inoperative or out of specification, follow the fault finding procedures outlined in paragraphs 5-14 to 5-17.

5-14. The self-check feature of the 9648M can often be used to trace a fault to the module or circuit level before the instrument is even removed from its combination case. Use the SEP-COM-CHK switch in CHK POSITION to couple the 1 MHz self-check signal to both Channels A and B. The accessary BNC to BNC cable supplied can be used to couple the 10 MHz CLOCK output to the Channel C input for checking FREQ C. Compare the resultant display in each mode of operation with the specified display contained in the performance check of 3-6. Note carefully which modes of operation are satisfactory and which are not, and use the troubleshooting aids of Table 5-4 to locate the faulty module or circuit.

5-15. After the instrument is removed from its combination case, always verify proper power supply operation before substituting modules or circuit tracing. Use an oscilloscope to check the Test point voltages against the limits listed in Table 5-5.

5-16. Carefully examine the instrument and check for any visual evidence of trouble. Check for broken wires, burned resistors, loose components, shorts or open or defective solder joints on the printed circuit boards. Check for separation of printed circuit board lands and pads. Check for open, defective, or intermittent switches. Check that connectors are clean and will mate properly.

5-17. Understand and be familiar with the circuit theory of Section IV. Refer to the functional block diagram, Figure 4-1 and the simplified schematic diagrams in Section IV and VI to isolate the probable circuit areas which may cause the problem. For a more detailed analysis of a particular circuit refer to the complete schematics in Section VI. Table 5-4 gives some probable remedies for specific symptoms.

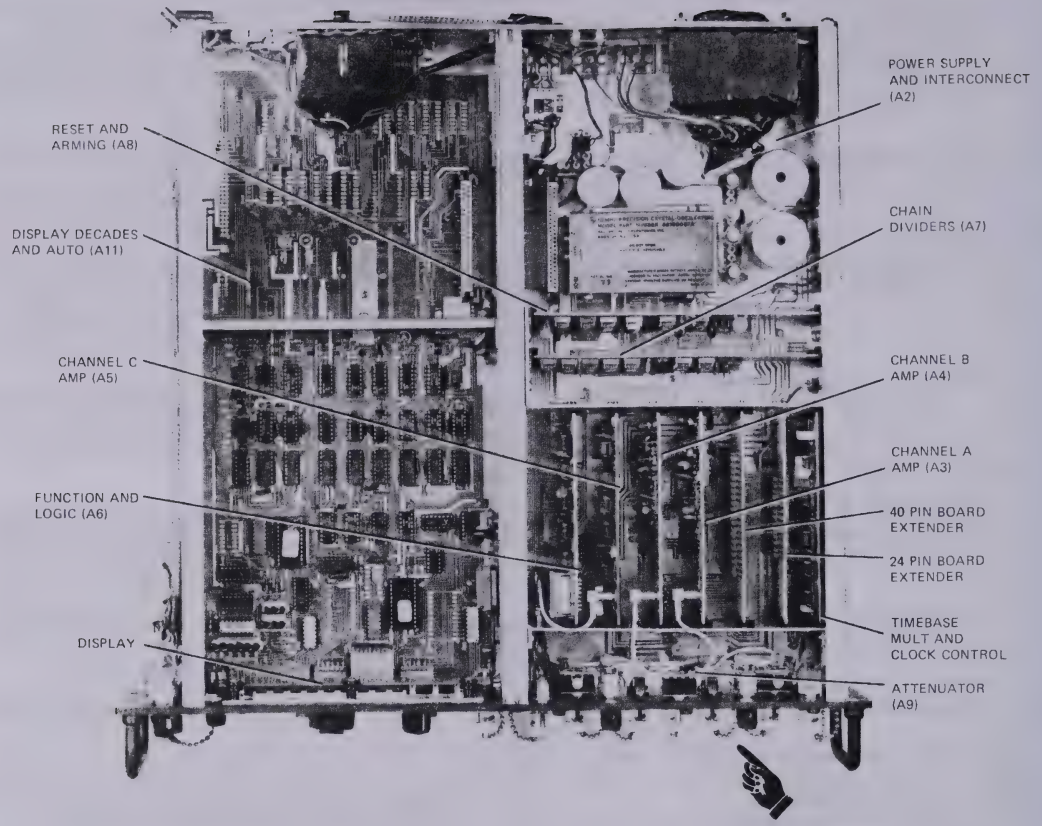



Figure 5-1. AN/USM-326A Board Location

5-18. PRINTED CIRCUIT BOARD REMOVAL. Refer to Figure 5-1.

5-18-1. DISPLAY BOARD. Unscrew the three No. 4-40 phillips head screws that secure the Display Board retainer bushings and remove the bushings. Disconnect the flexible printed circuit cable from connector A16 on the Display Decades and Auto printed circuit board. Disconnect the Display Board from connector J12 and remove it from the instrument. To install the Display Board, reverse the procedure.

5-18-2. FUNCTION AND LOGIC BOARD. Unscrew the No. 6-32 screw and remove the printed circuit board retainer. Unlatch the connector clamp and disconnect the 16 pin connector from J2 on the Function and Logic Board. Pull the board up from socket J10 and remove it from the instrument. Install the Function and Logic Board by reversing the procedure.

5-18-3. CHANNEL C AMP BOARD. Unscrew the No. 6-32 screw and remove the printed circuit board retainer. Unplug the coaxial cable from J1 on the Channel C Amp Board. Pull the board up from socket J9 and remove it from the instrument. Install the Channel C Amp Board by reversing the procedure.

5-18-4. CHANNEL B AMP BOARD. Follow the same procedure as described in 5-18-3.

5-18-5. CHANNEL A AMP BOARD. Follow the same procedure as described in 5-18-3.

5-18-6. TIME BASE MULT AND CLOCK CONTROL BOARD. Unscrew the No. 6-32 screw and remove the printed circuit board retainer. Pull the board up from J4 and remove it from the instrument. Install the Time Base Mult and Clock Control Board by reversing the procedure.

5-18-7. CHAIN DIVIDER BOARD. Follow the same procedure as described in 5-18-6.

5-18-8. RESET AND ARMING BOARD. Follow the same procedure as described in 5-18-6.

5-19. ALIGNMENT AND CALIBRATION

5-20. GENERAL. The following paragraphs describe procedures for adjusting the AN/USM-326A. Adjustment requires that the UNIVERSAL COUNTER be removed from its case. This is done by carefully following the steps outlined in 5-20-1.

WARNING

With the AN/USM-326A removed from its case and primary power applied, hazardous voltages are exposed which can cause personal injury. Observe all safety precautions.

Before proceeding with any calibration adjustments, all troubleshooting and related maintenance should be completed. Use a JFD alignment tool, No. 5284 or equivalent for all adjustments. The trimmer capacitors used in the oscillator are limited to a maximum torque of 10 inch-ounces. For the location of adjustments refer to Fig. 5-3.

5-20-1. REMOVAL FROM THE COMBINATION CASE

a. Disconnect the power cable from the front panel connector.

b. Loosen the sixteen slotted thumb screws located on the periphery of the front panel.

c. Place the instrument on the floor or bench with the front panel upright.

d. Pull the chassis straight up, slowly, by the two front panel handles until the back panel is free of the retaining pins.

e. Shift the chassis to the right side of the case and then pull it completely from the case.

f. To install the chassis back in the combination case, reverse the procedure.

5-21. OSCILLATOR CALIBRATION

NOTE

It is recommended that the AN/USM-326A be operating continuously for 24 hours prior to performing this adjustment.

a. Check that the INT-EXT CLOCK switch on the rear panel of the 6130A (AN/USM-441) Time Mark Generator is in the EXT CLOCK IN position.

b. Connect the 10 MHz frequency standard to the INT-EXT BNC connector on the rear panel of the 6130A.

c. Set the HIGH FREQUENCY switch of the 6130A to 2 ns.

d. Connect 50 Ω BNC to BNC cable from the H.F. OUT BNC connector on the 6130A to the C INPUT BNC connector on the AN/USM-326A.

e. Set the FUNCTION switch to FREQ C and TIME BASE/RESOLUTION to 10 s on the AN/USM-326A.

f. Remove the seal screw from the FREQUENCY ADJUST FINE access hole, accessible through hole in extruded partition. Insert the alignment tool and slowly adjust until display indicates 500000000.0 Hz ±1 count. Several incremental adjustments are recommended, waiting about 10 minutes between each adjustment for the oscillator to stabilize.

g. If there is insufficient range in the FINE adjustment, re-set the FINE trimmer to mechanical center and make the first adjustment with the FREQUENCY ADJUST COARSE trimmer located adjacent to the FINE trimmer capacitor.

h. Repeat step f.

5-22. CHANNEL A DC BAL ADJUSTMENT

a. Set the front panel controls as outlined in 5-9-1a, except SAMPLE RATE fully clockwise, TIME BASE/RESOLUTION to 1 s and SEP-COM-CHK to CHK.

b. Adjust Channel A DC BAL, using the JFD alignment tool, for a stable display of 1000000 Hz ±1 count.

c. Connect the terminated output of the Tektronix 191 Signal Generator to Channel A INPUT of the AN/USM-326A.

d. Change TIME BASE/RESOLUTION to AUTO 6DGT and SEP-COM-CHK to SEP.

e. Set the 191 generator frequency to 100 MHz and level to 150 mV p-p. Re-adjust Channel A DC BAL for a stable display of approximately 100.000 MHz.

f. Continuously decrease 191 generator signal and re-adjust DC BAL until no further increase in sensitivity is obtained.

g. Change the 191 generator frequency to 50 kHz and check that display remains stable.

h. Using the Model 3028A Digital Multimeter, measure the voltage between pin 7 of 24 pin attenuator connector and ground. Refer to Figure 5-4. Check that when Channel A TRIG LEVEL control is varied between PRESET and full clockwise rotation, the voltage on the wiper swings at least ±2.5V.

5-23. CHANNEL B DC BAL ADJUSTMENT

a. Set the front panel controls as follows:

| | |
|---|---|
| SAMPLE RATE | Full CW |
| FUNCTION | RATIO A/B |
| TIME BASE/RESOLUTION | 1 s |
| ⌐, ¬ (Slope, Channel B) | + |
| DC/AC/LF (Channel B) | DC |
| X1/X10/X100 (Channel B) | X1 |
| SEP-COM-CHK | CHK |
| STORAGE | ON |
| CLOCK | INT OUT |
| ARM | OFF |

b. Adjust Channel B DC BAL, using the JFD alignment tool, for a stable display of 1.000000.

c. Using the BNC to BNC test cable supplied, connect the CLOCK output BNC to Channel A INPUT BNC. Change Channel A coupling switch to AC and Channel A attenuation to X10. Change SEP-COM-CHK switch to COM. Check for a stable display of 1.000000 ±1 count.

d. Switch the Channel A attenuator to X100 and check that display remains stable at 1.000000 ±1 count.

e. Using the Model 3028A Digital Multimeter, measure the voltage between pin 5 of 24 attenuator connector and ground. Check that when Channel B TRIG LEVEL control is varied between PRESET and full clockwise rotation, the voltage on the wiper swings at least ±2.5V.

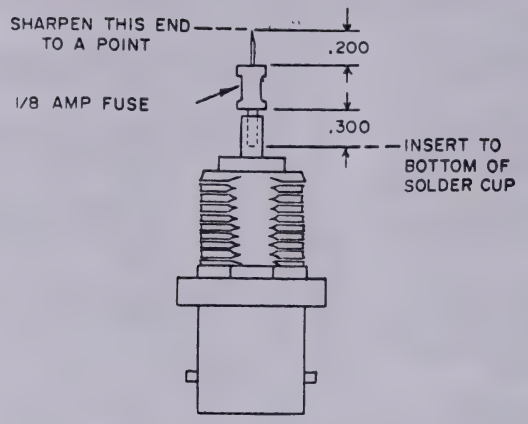
f. Remove the BNC to BNC test cable.

Table 5-4. Troubleshooting Procedures

| TROUBLE | PROBABLE CAUSE/REMEDY |
|---|---|
| 1. OVN indicator does not illuminate when power switch is in STDBY. | 1. AC power cord not inserted or connected. Check oven circuit fuse on rear panel. Check the following on the A2 power supply board: TP9 +18V unreg. (19 to 26 Volts). -If incorrect, check CR1, CR2, C7. TP2 +12V (11.4V to 12.6V). -If incorrect check U2 12 Volt regulator. |
| 2. OVN indicator illuminates, display does not illuminate when power switch is ON and when DISPLAY TEST is depressed. | 2. Check main fuse on front panel. Check the following on DISPLAY DECADES board. TP1+5V (4.75 to 5.25V), TP+5V (4.75 to 5.25V). If incorrect, check A2 CR4, A2 CR5, A2 C11, A11 U59, A11 U58. |
| 3. One or more digits does not illuminate when DISPLAY TEST is depressed. | 3. TIME BASE/RESOLUTION switch not in 9DGT or manual position. Check A11 U2, A11 U3, A11 RN1. Substitute Display board. |

Table 5-4. Troubleshooting Procedures (Cont)

| TROUBLE | PROBABLE CAUSE/REMEDY |
|---|---|
| 4. One or more segments missing from each digit. | 4. Check A11 U24, A11 RN2. |
| 5. Unit operates only in Ratio A/B, Ratio C/B, and totalizes modes. | 5. Substitute CLOCK and TBM board. Substitute FUNCTION board. |
| 6. Unit operates only in ELAPSED TIME, RATIO C/B and FREQ C modes. | 6. Substitute Ch. A Amp. board. Substitute Ch. C Amp. board. Substitute FUNCTION board. |
| 7. Unit operates only in ELAPSED TIME mode. | 7. Substitute Ch. C Amp. board. Substitute FUNCTION board. Check +5V at A2 TP3 (4.75 to 5.25V). |
| 8. Unit does not operate in TIME INTVL A→B or any RATIO Mode. Operates in all other modes. | 8. Substitute Ch. B Amp. board. Substitute FUNCTION board. |
| 9. Unit does not operate in FREQ C or RATIO C/B modes. Operates in all other modes. | 9. Check Ch. C input fuse (front panel). Refer to Figure 5-2 for Channel C fuse preparation. Substitute Ch. C Amp. board. Substitute FUNCTION board. Check A2 TP1 -5 Volts (-4.75 to -5.25V). |
| 10. Unit does not operate in all TIME BASE/RESOLUTION control positions. | 10. Substitute CHAIN DIVIDERS board. |
| 11. Unit does not operate with external time base. | 11. Substitute CLOCK & TBM board. |
| 12. Storage function inoperative. | 12. Substitute RESET & ARMING board. Check front panel STORAGE switch. |
| 13. ARM function inoperative. | 13. Substitute RESET & ARMING board. Check front panel ARM switch. |
| 14. Unit updates display only if RESET switch is depressed. | 14. Check that SAMPLE RATE control is not in HOLD position. Substitute RESET & ARMING board. |
| 15. FREQ C mode operative at only certain frequencies. | 15. Substitute Ch. C Amp. board. |
| 16. Unit does not operate in PERIOD, ⎍, ⎎, TIME INTVL A→B and ELAPSED TIME modes. | 16. Substitute FUNCTION board. |
| 17. Display updates in TOTAL mode only, display holds reading in other modes even when RESET is depressed. | 17. Substitute RESET & ARMING board. |
| 18. Gate light flashes in FREQ A and FREQ C modes with no input applied. | 18. Substitute Ch. C Amp. board. |
| 19. Slope switch does not influence display in TIME INTVL A→B mode. | 19. Substitute CHAIN DIVIDERS board. Substitute RESET & ARMING board. |
| 20. FREQ A mode operative at only certain frequencies. | 20. Substitute Ch. A board. Substitute Ch. B board. |




NOTE: CHECK THAT FUSE IS PERPENDICULAR TO BNC CONNECTOR MOUNTING PLANE TO FACILITATE INSERTION INTO SOCKET.

Figure 5-2. Channel C Fuse Preparation

Table 5-5. Power Supply Test Points

| | | | |
|---|---|---|---|
| A. | Power Supply and Interconnect Board (A2) | | |
| | TEST POINT | VOLTAGE | LIMITS |
| | TP1 | -5V | -4.75 to -5.25 Volts |
| | TP2 | +12V | 11.4 to 12.6 Volts |
| | TP3 | +5V | 4.75 to 5.25 Volts |
| | TP4 | +5V | 4.75 to 5.25 Volts |
| | TP5 | -15V | -14.25 to 15.75 Volts |
| | TP6 | +15V | 14.25 to 15.75 Volts |
| | TP7 | 10 MHz Sine | 1V RMS minimum |
| | TP8 | +12V | 11.4 to 12.6 Volts |
| | TP9 | +18 unreg. | 18-21 Cold, 23-25 Volts after warm-up |
| B. | Display Decades and Auto Board (A11) | | |
| | TP1 | +5V | 4.75 to 5.25 Volts |
| | TP2 | +5V | 4.75 to 5.25 Volts |
| C. | Time Base Multiplier and Clock Board (A1) | | |
| | TP4 | +5V | 4.75 to 5.25 Volts |

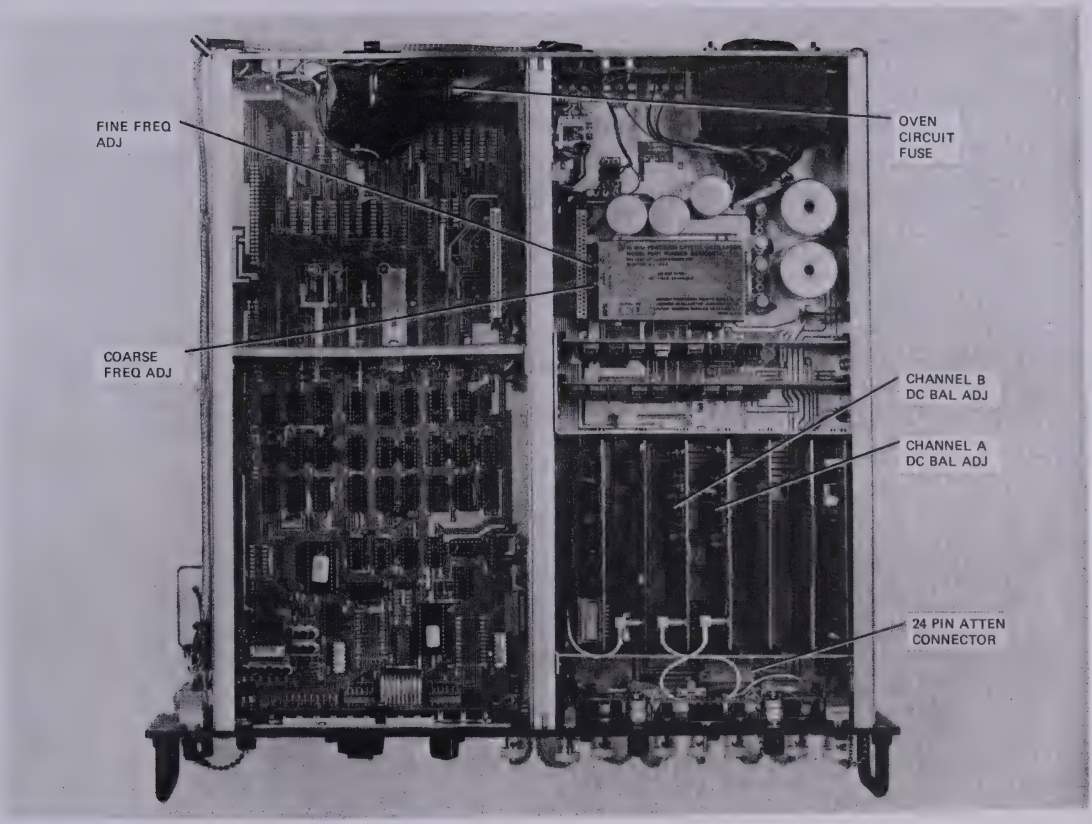
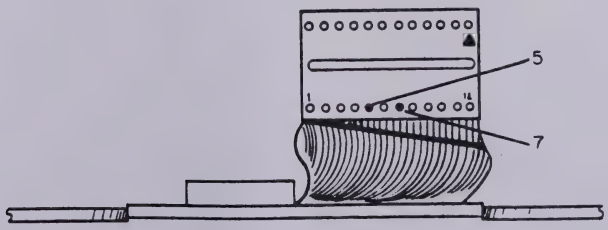



Figure 5-3. Adjustment Locations




24 PIN ATTENUATOR CONNECTOR

Figure 5-4. 24 Pin Attenuator Connector

# SECTION VI

# DIAGRAMS

## 6-1. GENERAL

6-2. This section contains the circuit diagrams referenced throughout other sections of the manual. Included are two of the simplified schematics referred to in Section IV, Theory of Operation.

6-3. Each circuit diagram is identified by a figure number, the nomenclature of the assembly which the circuit diagram represents and the reference designation of the assembly.

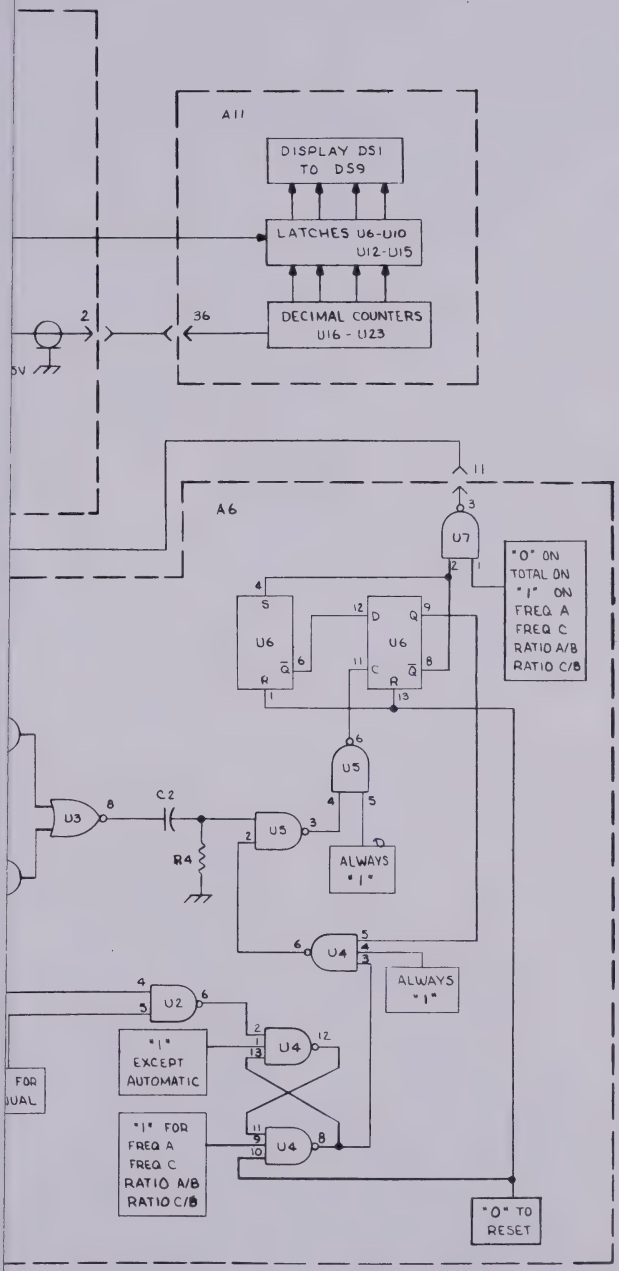



**Figure 6-1. Simplified Schematic Total, Frequency and Ratio Circuits**

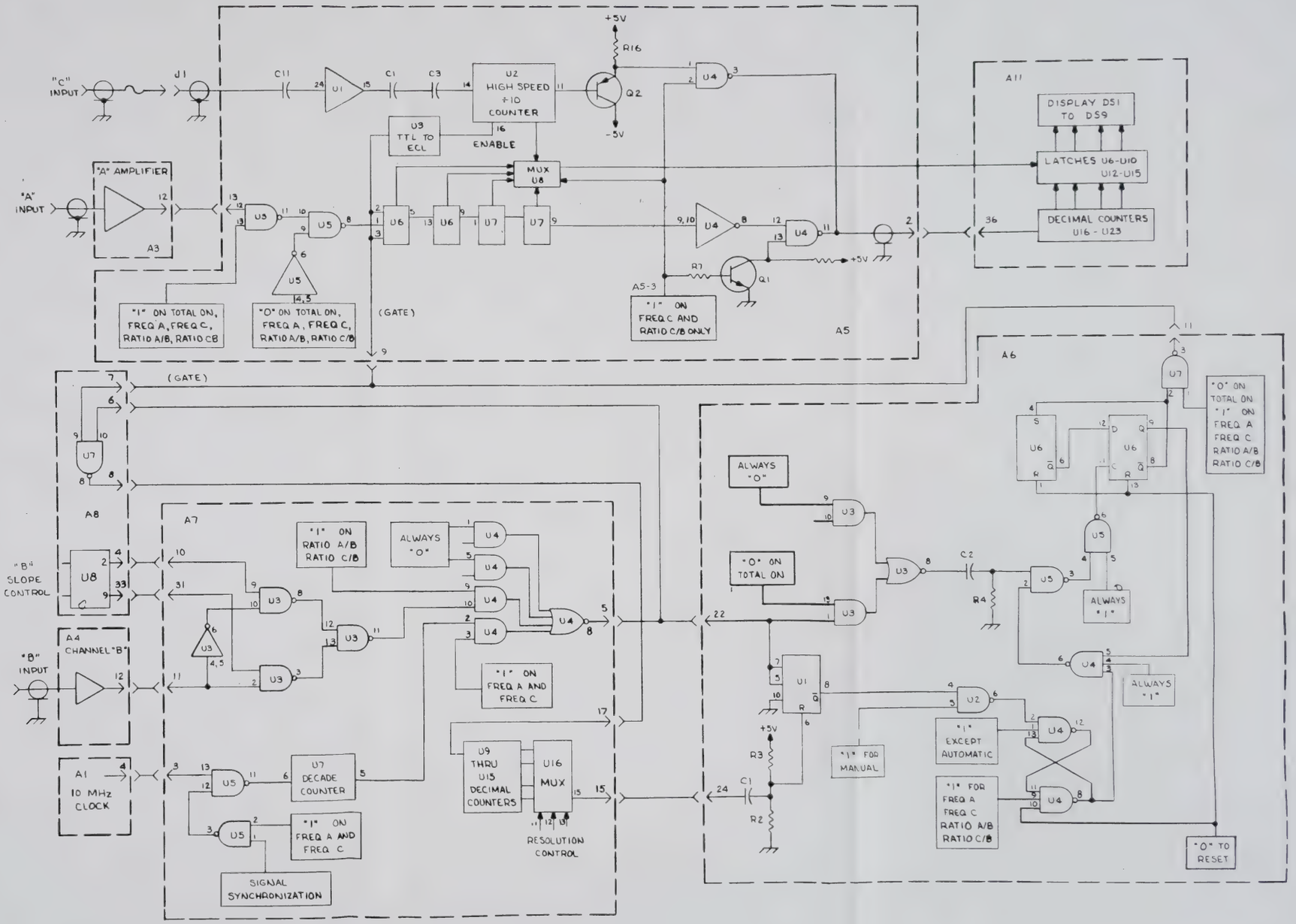



Figure 6-1. Simplified Schematic Total, Frequency and Ratio Circuits

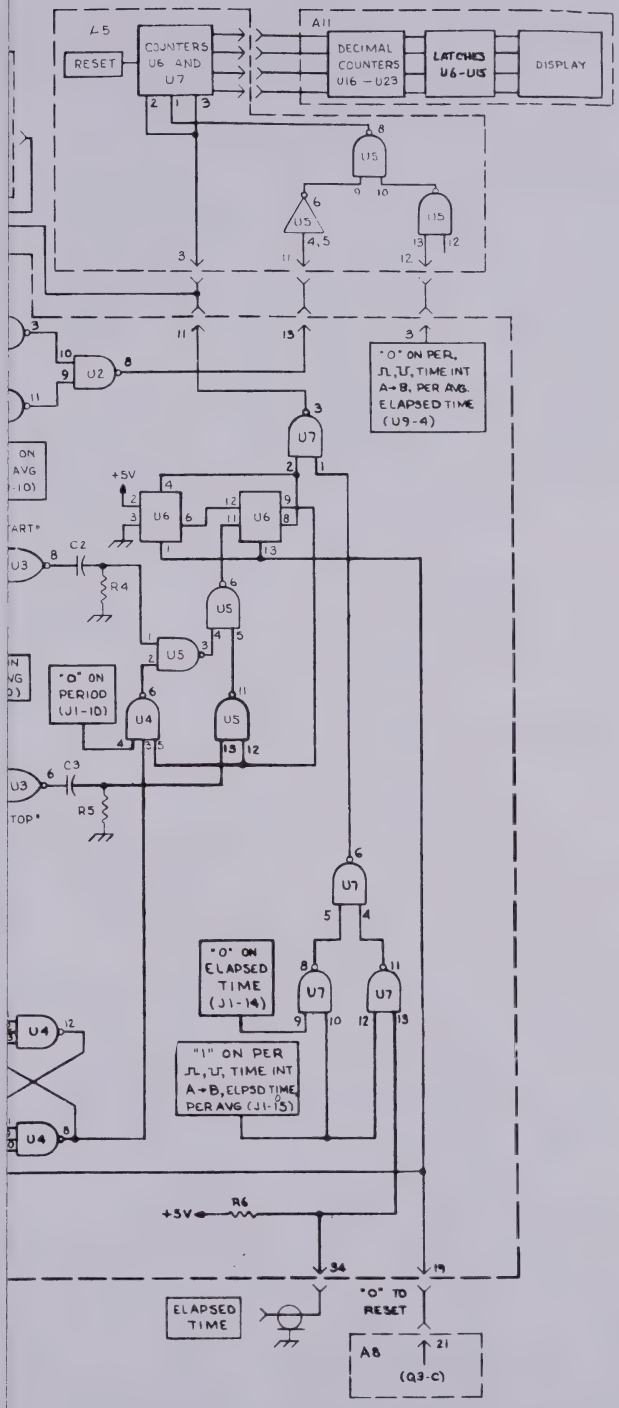



Figure 6-2. Simplified Schematic Time Function Circuits

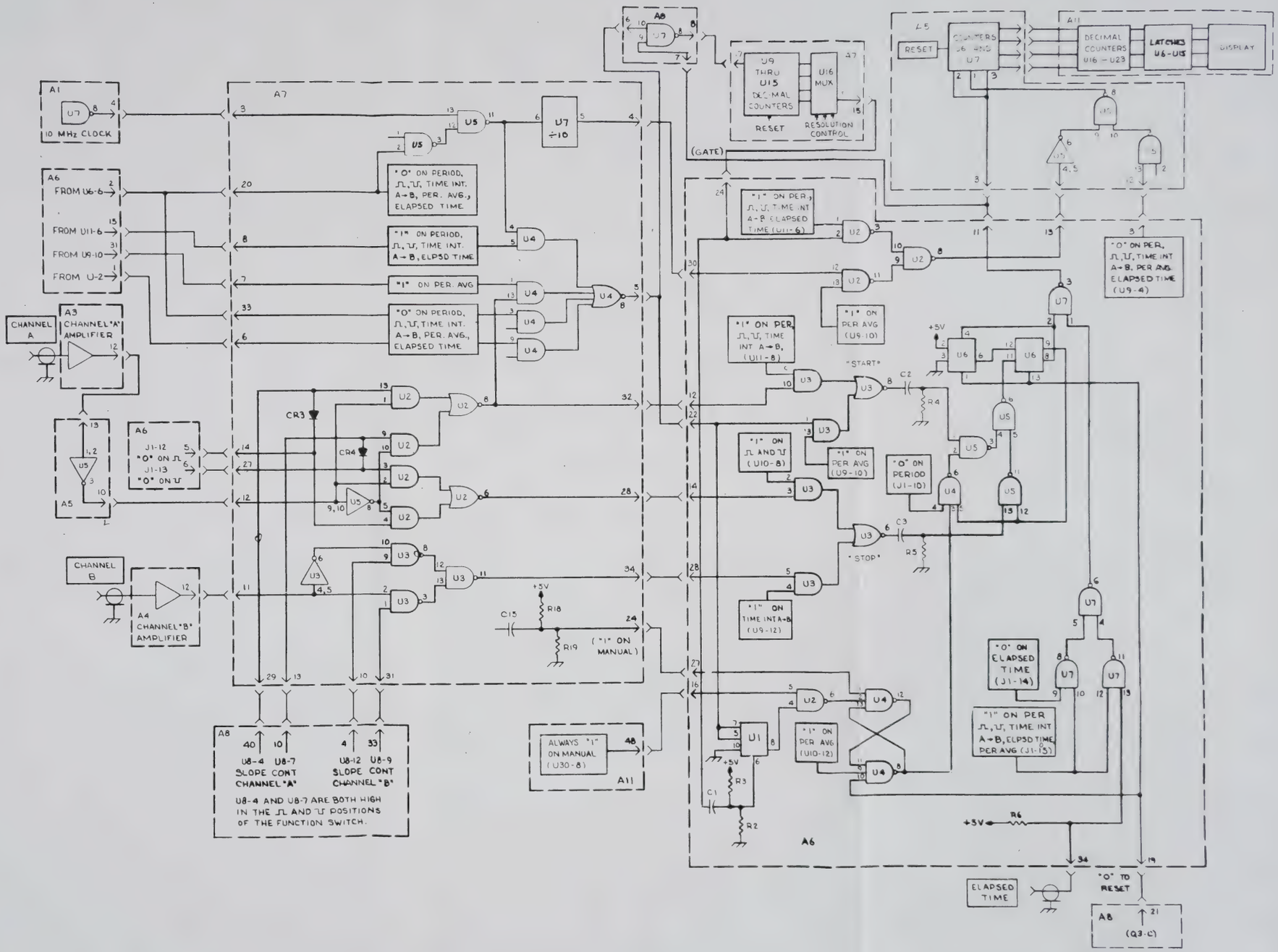



Figure 6-2. Simplified Schematic Time Function Circuits

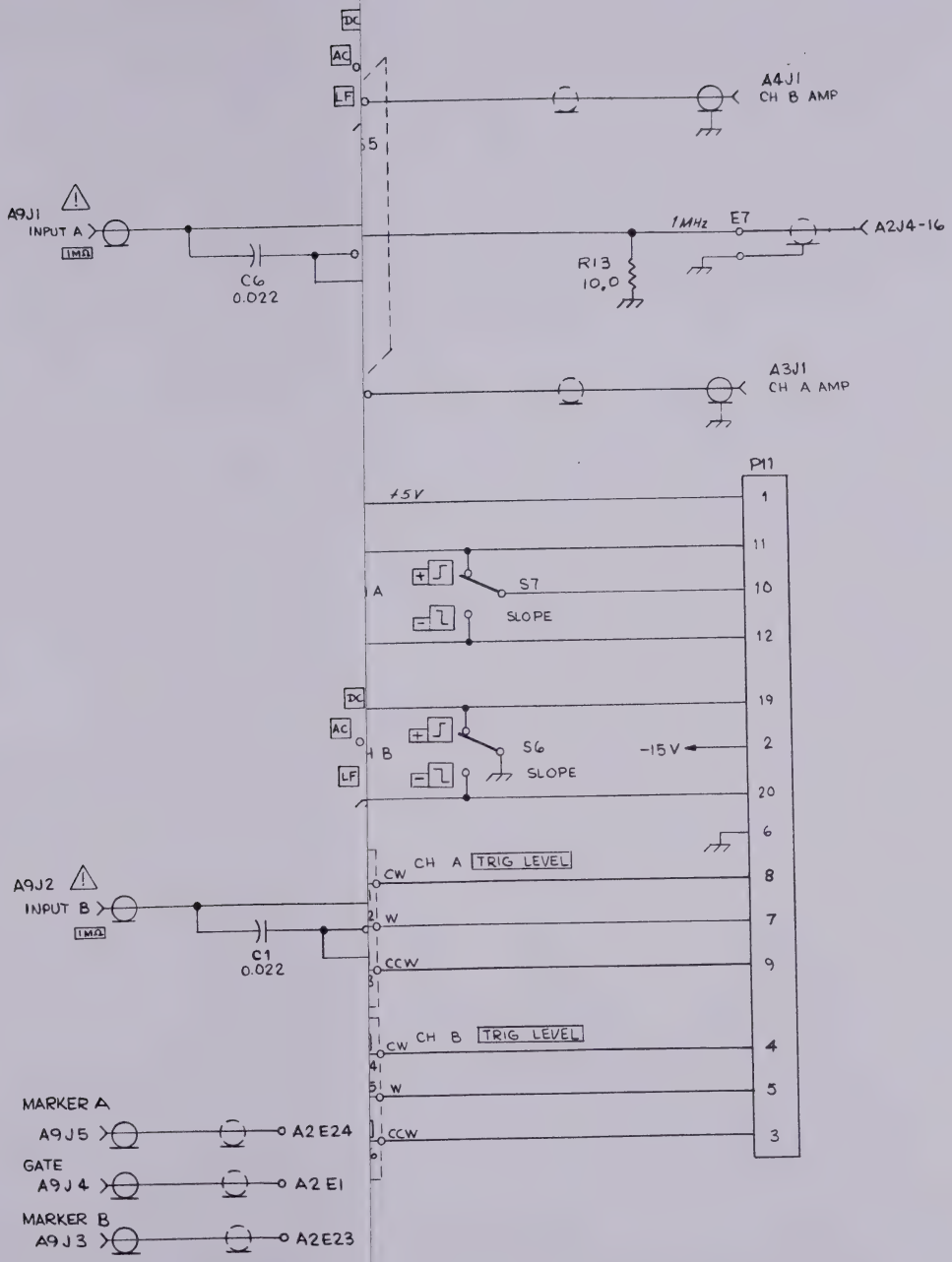
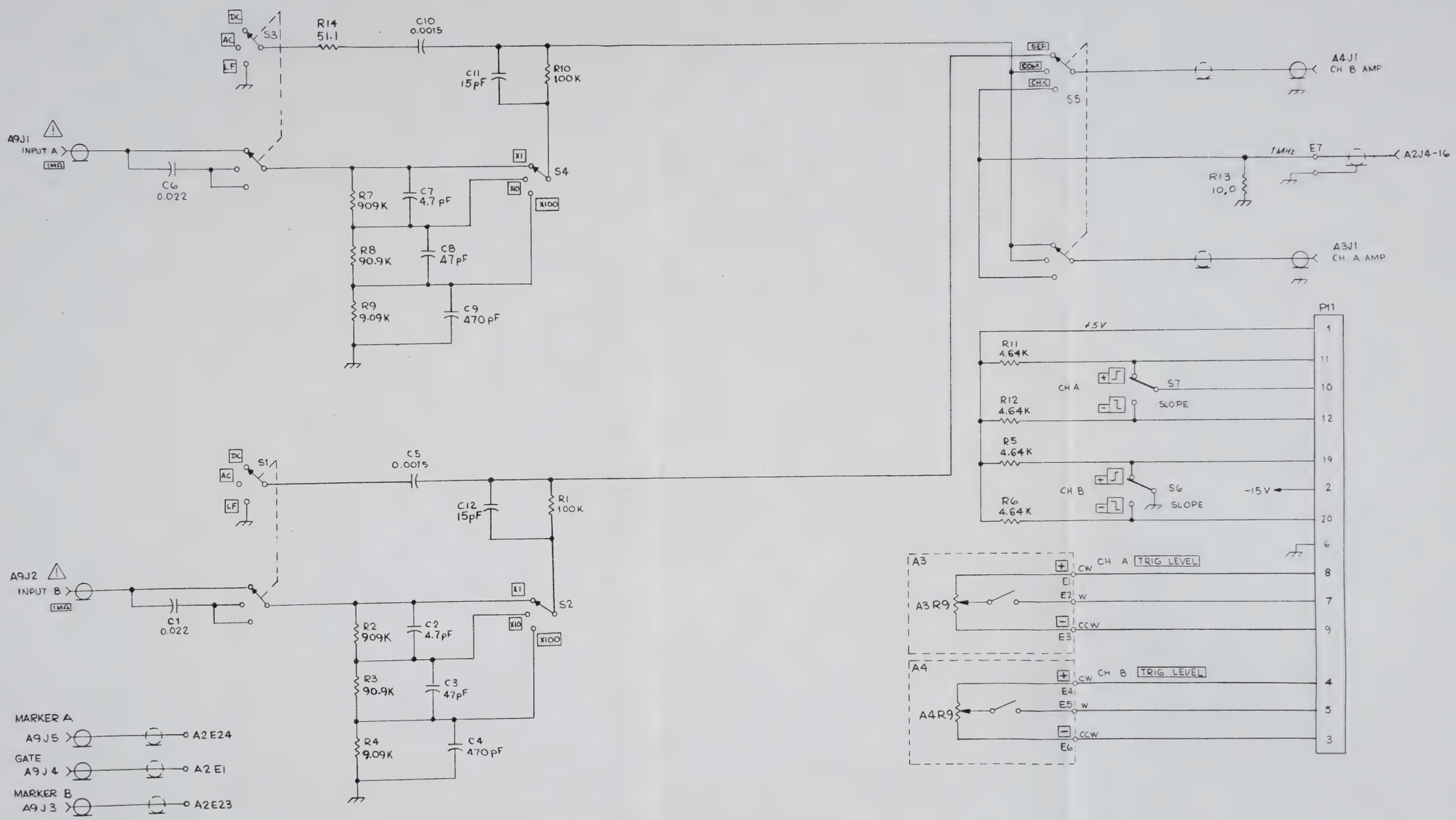


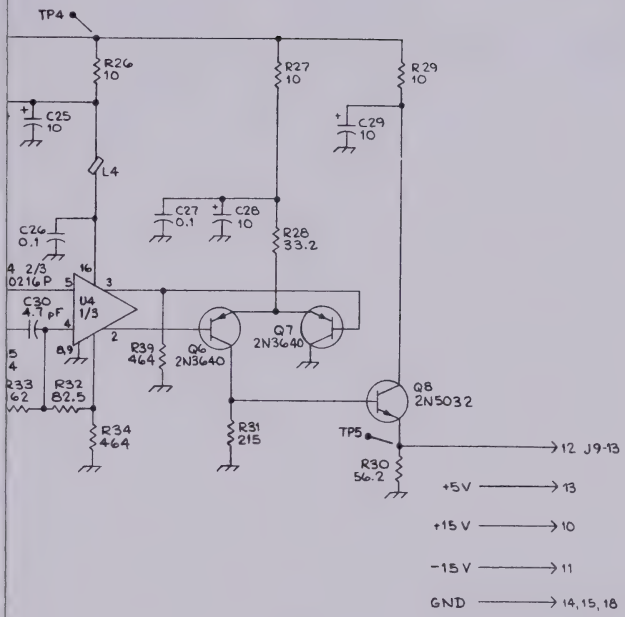

Figure 6-3. Attenuator Assembly A9, Circuit Diagram




NOTES:

1. ALL CAPACITANCE VALUES ARE IN MICROFARADS AND ALL RESISTANCE VALUES ARE IN OHMS UNLESS NOTED OTHERWISE.

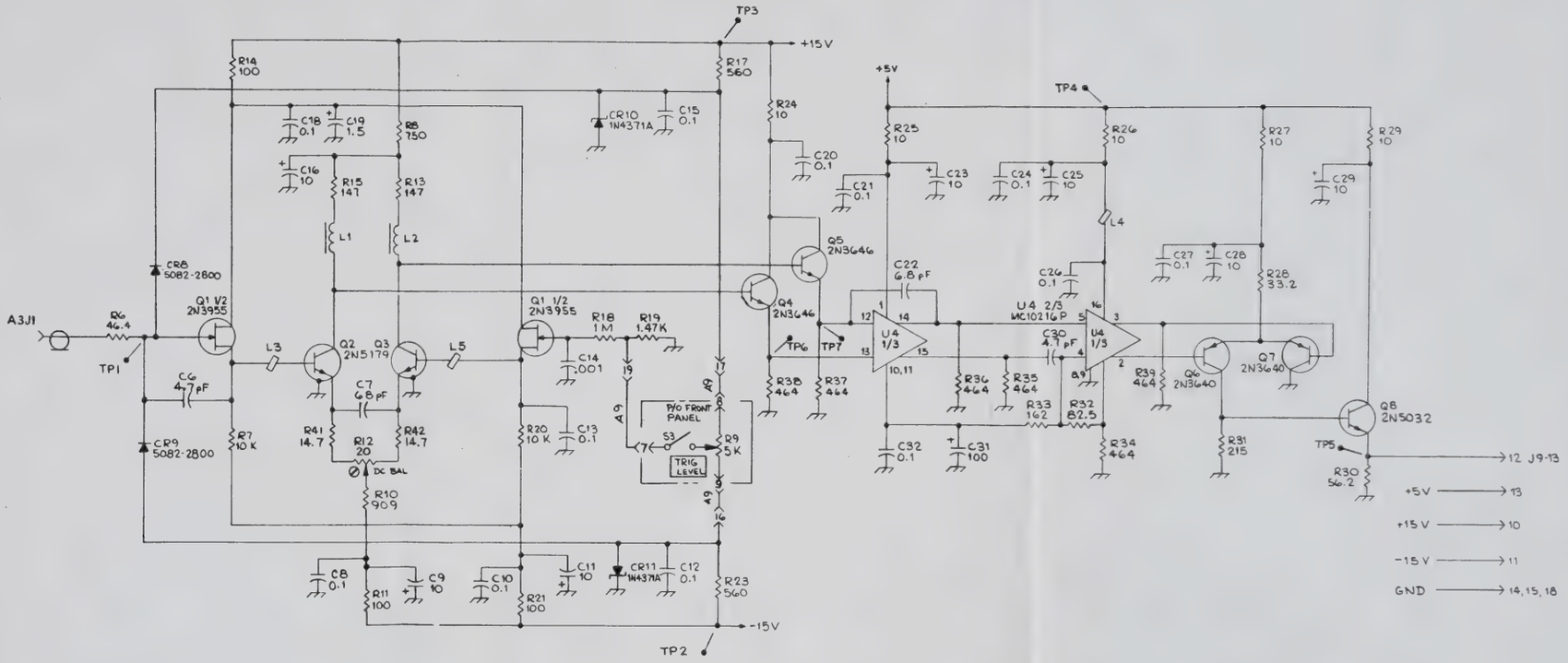
**Figure 6-3. Attenuator Assembly A9, Circuit Diagram**




ARE IN MICROFARADS AND
ARE IN OHMS.

A3P7.

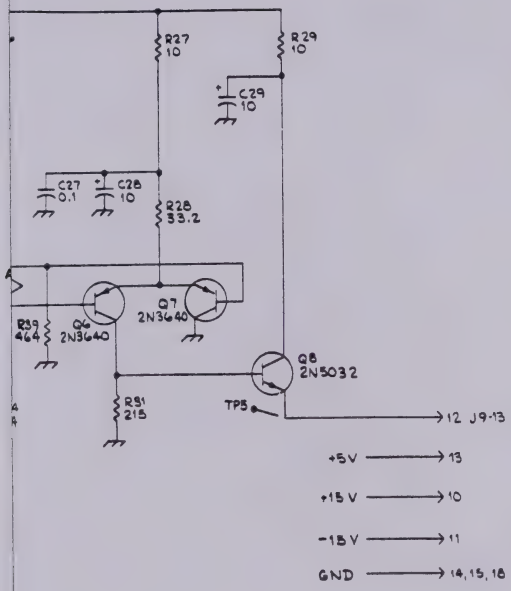
Figure 6-4. Channel A Assembly A3, Circuit Diagram




NOTES:

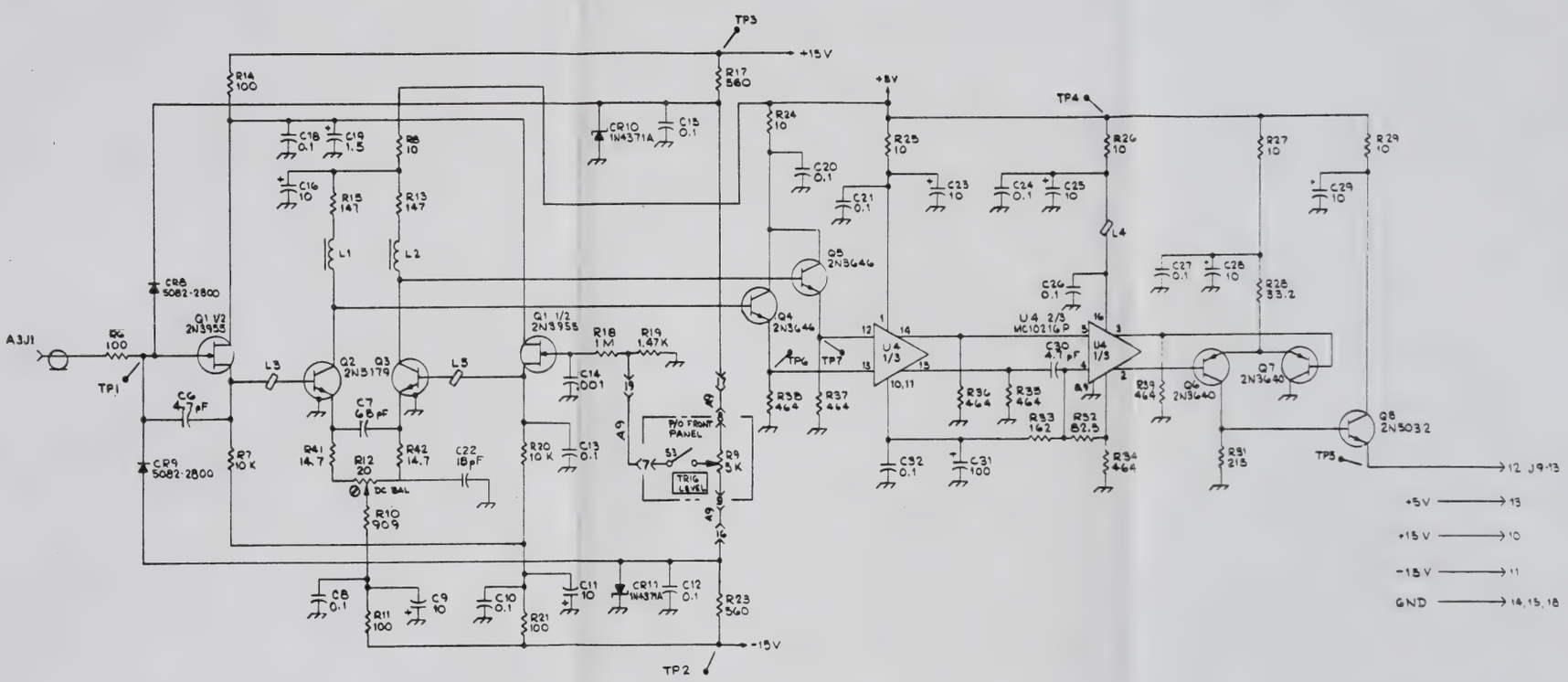
1. ALL CAPACITANCE VALUES ARE IN MICROFARADS AND ALL RESISTANCE VALUES ARE IN OHMS.
2. ⟵ DENOTES CONTACT OF A3P7.

**Figure 6-4. Channel A Assembly A3, Circuit Diagram**




ARADS AND

Figure 6-4A. Channel A Assembly A3, Circuit Diagram (Serial No. 526 and Above)

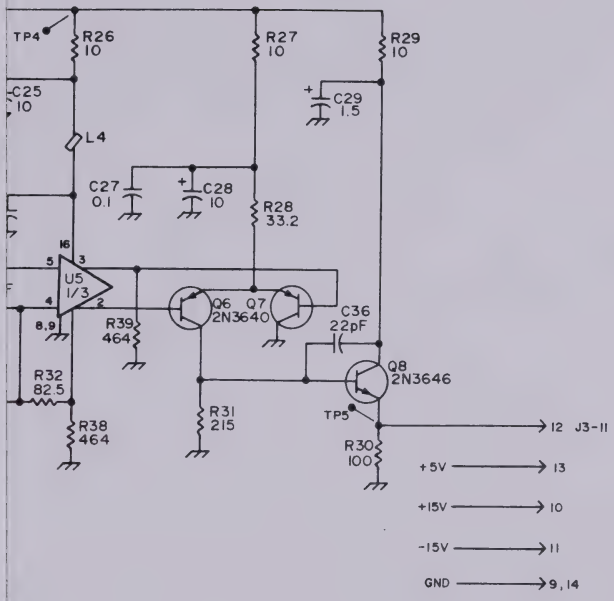



NOTES:

1. ALL CAPACITANCE VALUES ARE IN MICROFARADS AND ALL RESISTANCE VALUES ARE IN OHMS.
2. ← DENOTES CONTACT OF A3P7.

Figure 6-4A. Channel A Assembly A3, Circuit Diagram (Serial No. 526 and Above)

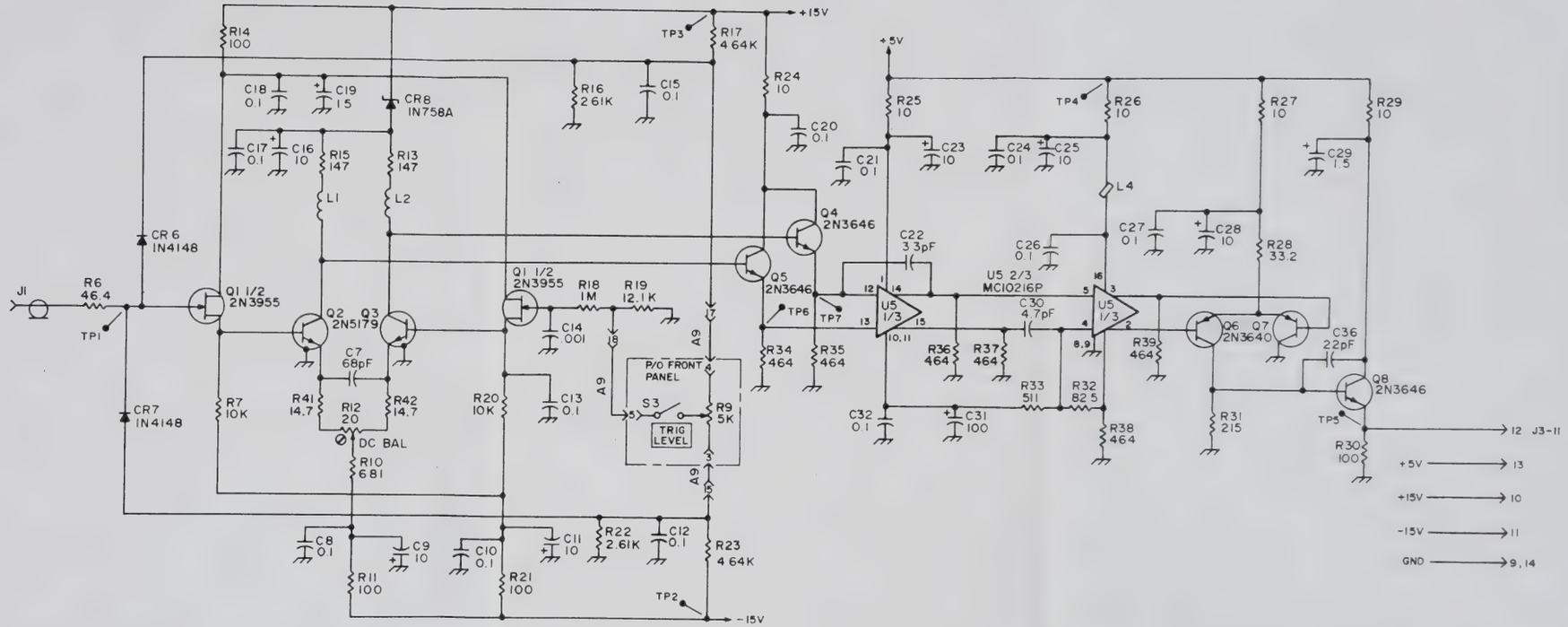
6.00 sup 5-1




IN MICROFARADS AND
N OHMS.

P8.

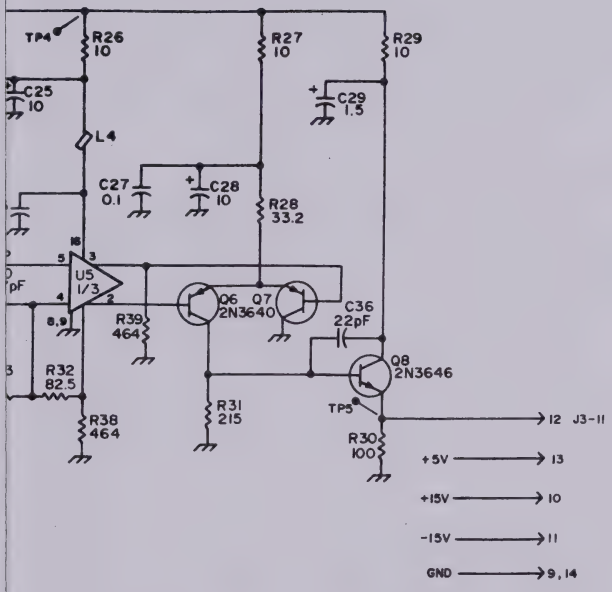
Figure 6-5. Channel B Assembly A4, Circuit Diagram




NOTES:

1. ALL CAPACITANCE VALUES ARE IN MICROFARADS AND ALL RESISTANCE VALUES ARE IN OHMS.
2. ⟵ DENOTES CONTACT OF A4P8.

Figure 6-5. Channel B Assembly A4, Circuit Diagram

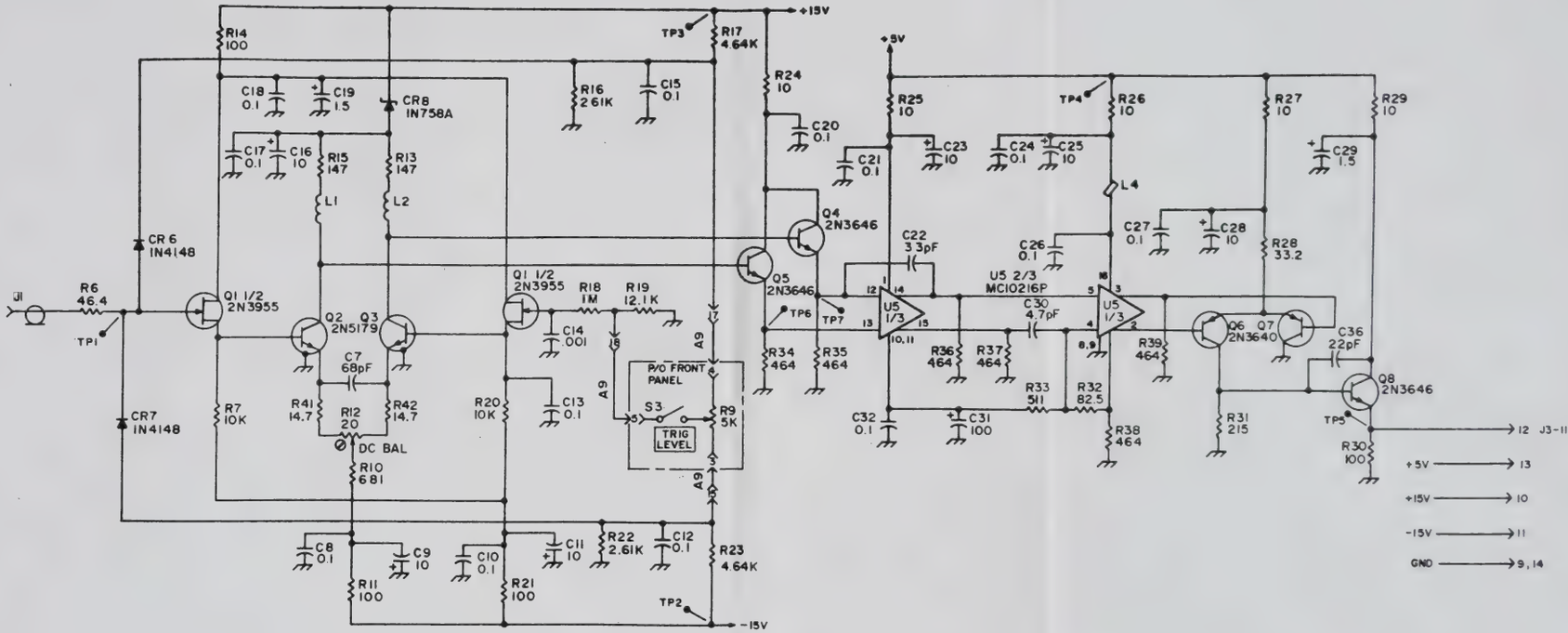



E IN MICROFARADS AND
E IN OHMS.

A4P8.

nel B Assembly A4, Circuit
N 92-10243-5Q

THE END




NOTES:

1. ALL CAPACITANCE VALUES ARE IN MICROFARADS AND ALL RESISTANCE VALUES ARE IN OHMS.
2. ← DENOTES CONTACT OF A4P8.

Figure 6-5. Channel B Assembly A4, Circuit P/N 92-10243-5Q

THE END

CAPACITANCE VALUES ARE IN MICROFARADS
ALL RESISTANCE VALUES ARE IN OHMS UNLESS
ED OTHERWISE.
-DENOTES CONTACT OF A5P9.
.3GHz AMPLIFIER, BLI P/N 24-10104-1A

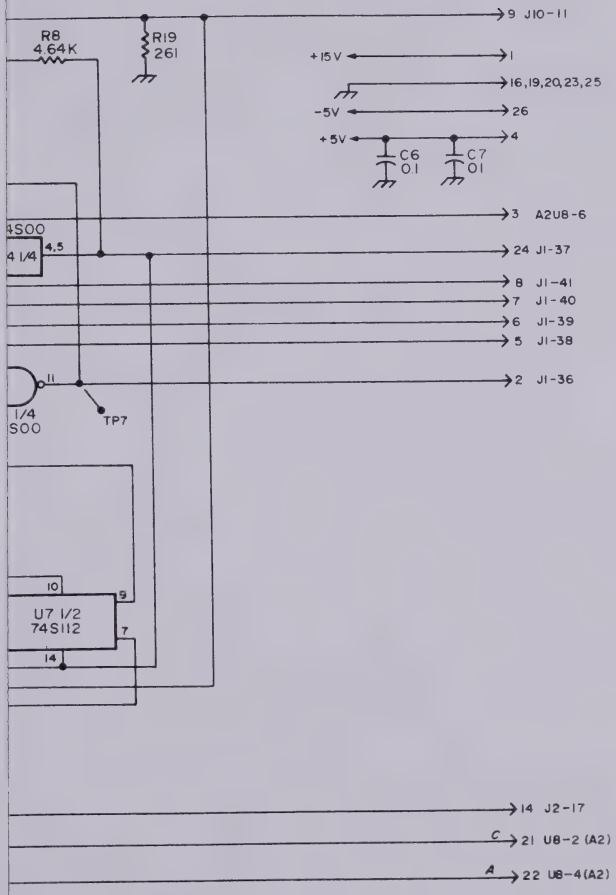



Figure 6-6. Channel C and High Speed Decade Assembly A5, Circuit Diagram

NOTES
1. ALL CAPACITANCE VALUES ARE IN MICROFARADS AND ALL RESISTANCE VALUES ARE IN OHMS UNLESS NOTED OTHERWISE
2. ⟵ DENOTES CONTACT OF A5P9.
3. U1, 1.3GHz AMPLIFIER, BLI P/N 24-10104-1A

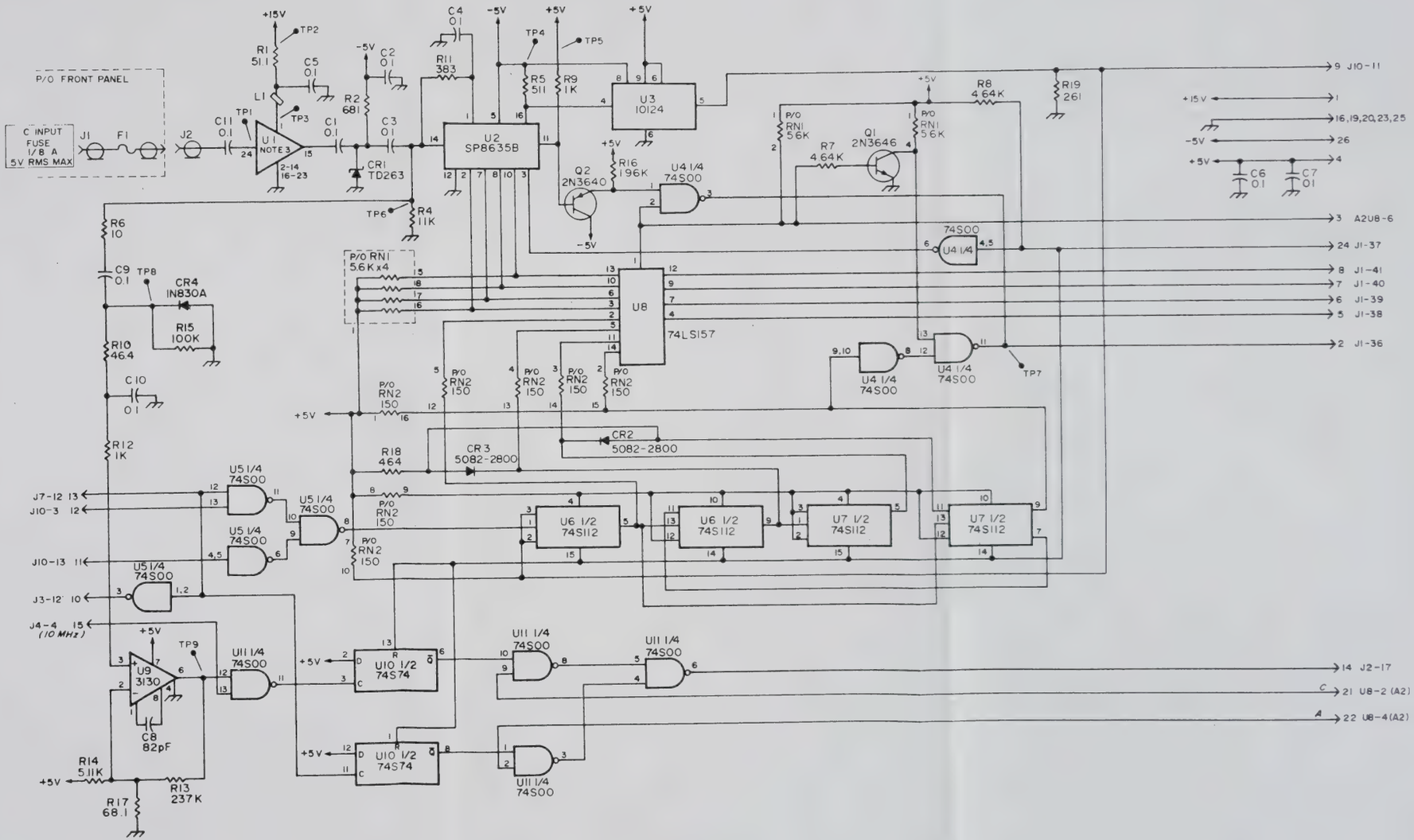



Figure 6-6. Channel C and High Speed Decade Assembly A5, Circuit Diagram

CE VALUES ARE IN MICROFARADS
TANCE VALUES ARE IN OHMS UNLESS
VISE

CONTACT OF A5P9.

PLIFIER. BLI P/N 24-10104-1A

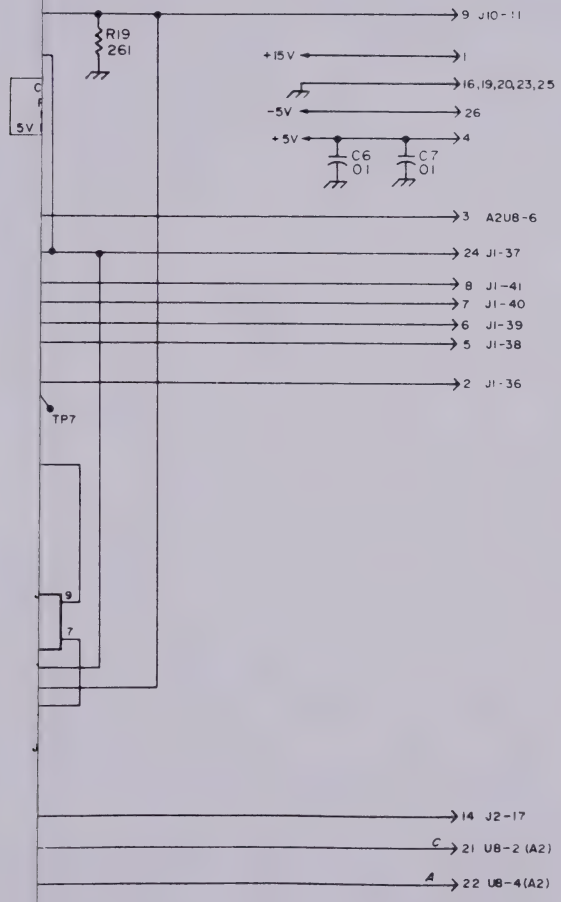



Figure 6-6A. Channel C and High Speed Decade Assembly A5, Circuit Diagram (Serial No. 526 and Above)

NOTES

ALL CAPACITANCE VALUES ARE IN MICROFARADS AND ALL RESISTANCE VALUES ARE IN OHMS UNLESS NOTED OTHERWISE

2 ← DENOTES CONTACT OF A5P9

3 UI, 1.3GHz AMPLIFIER, BLI P/N 24-10104-1A

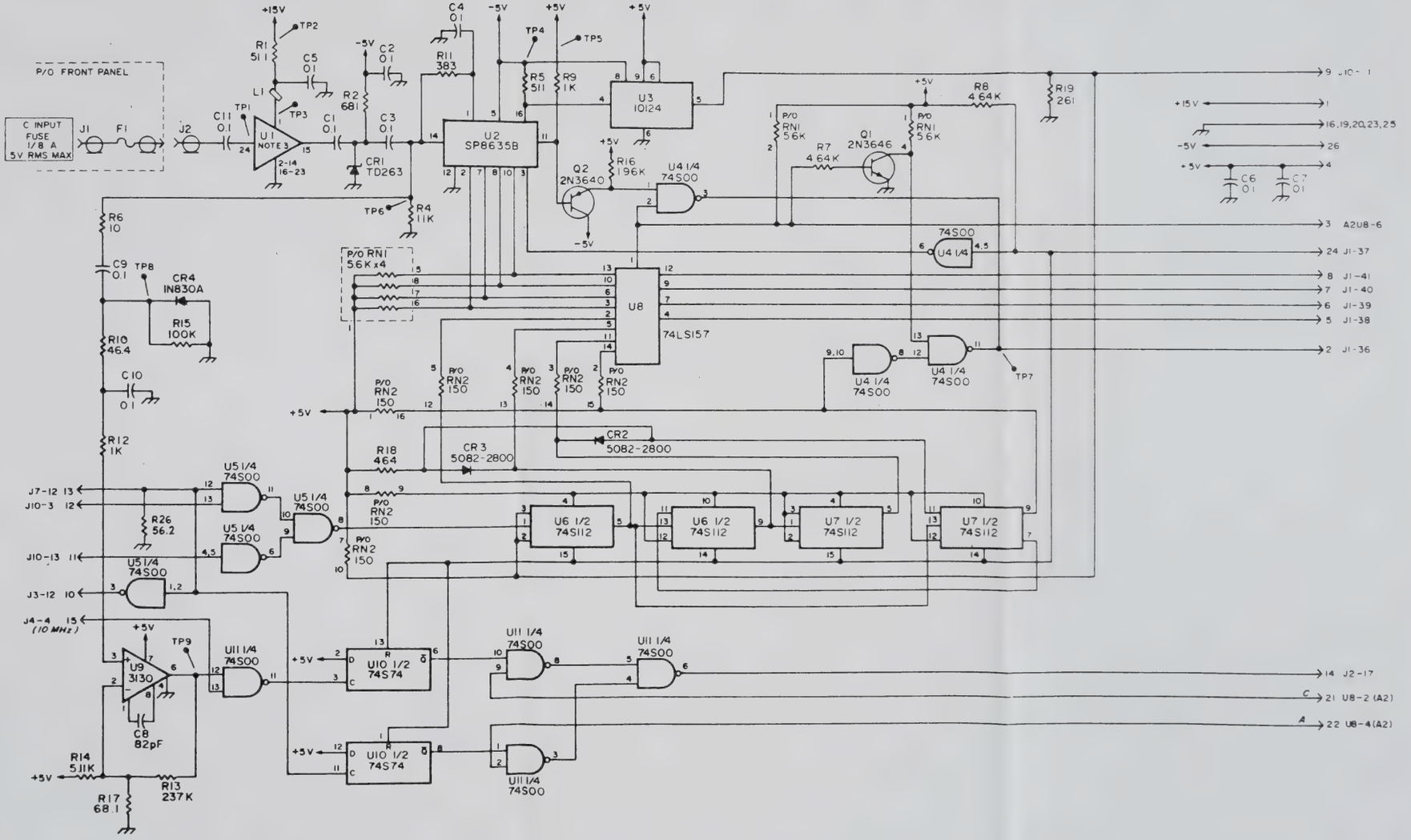



Figure 6-6A. Channel C and High Speed Decade Assembly A5, Circuit Diagram (Serial No. 526 and Above)

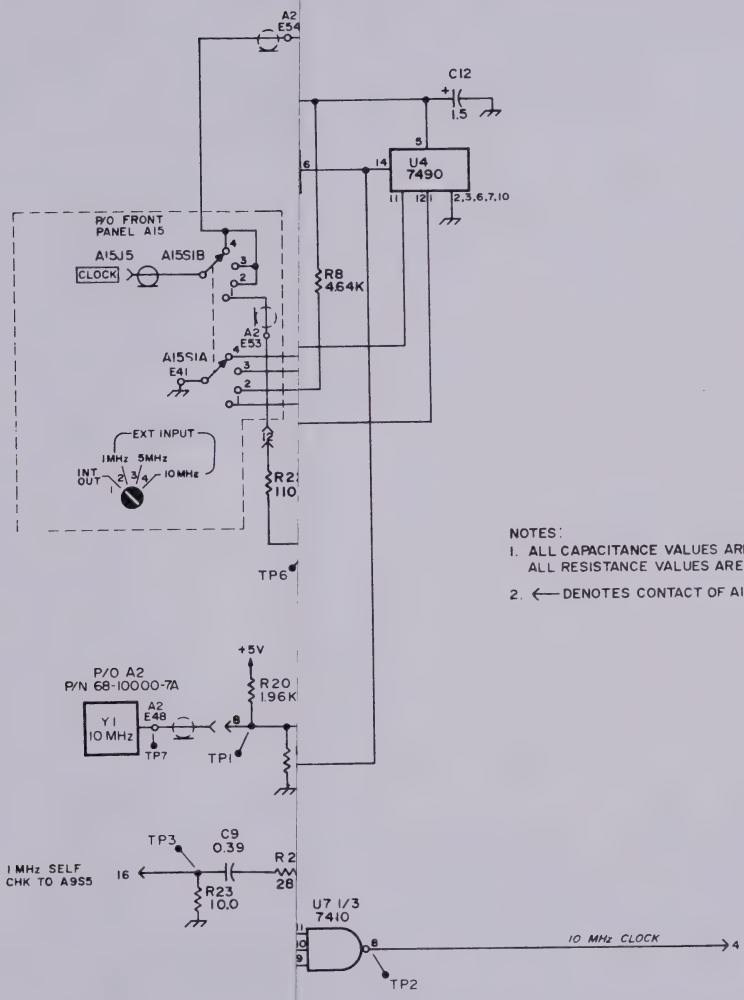



Figure 6-7. Time Base Multiplier and Clock Control Assembly A1, Circuit Diagram

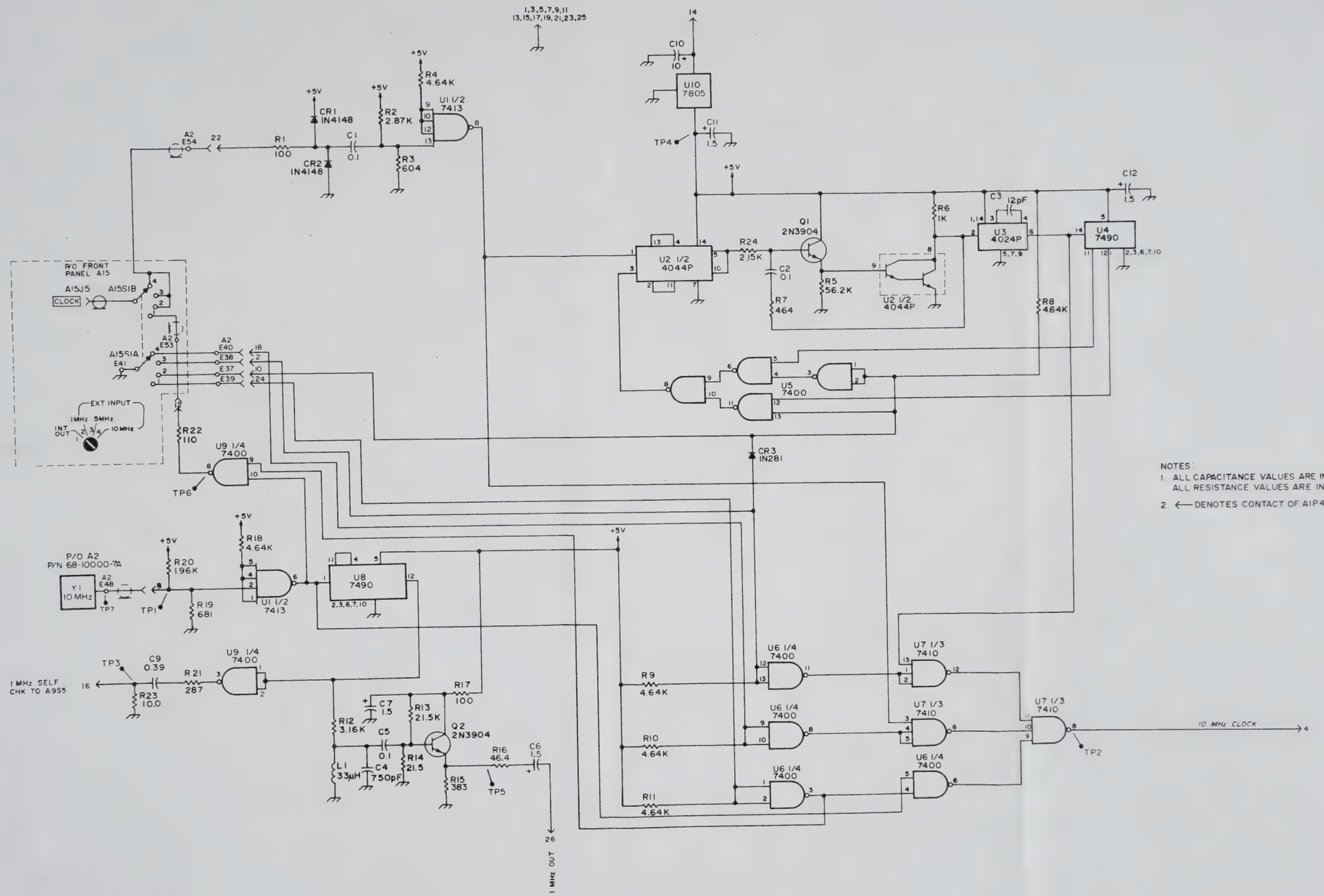



Figure 6-7. Time Base Multiplier and Clock Control Assembly A1, Circuit Diagram

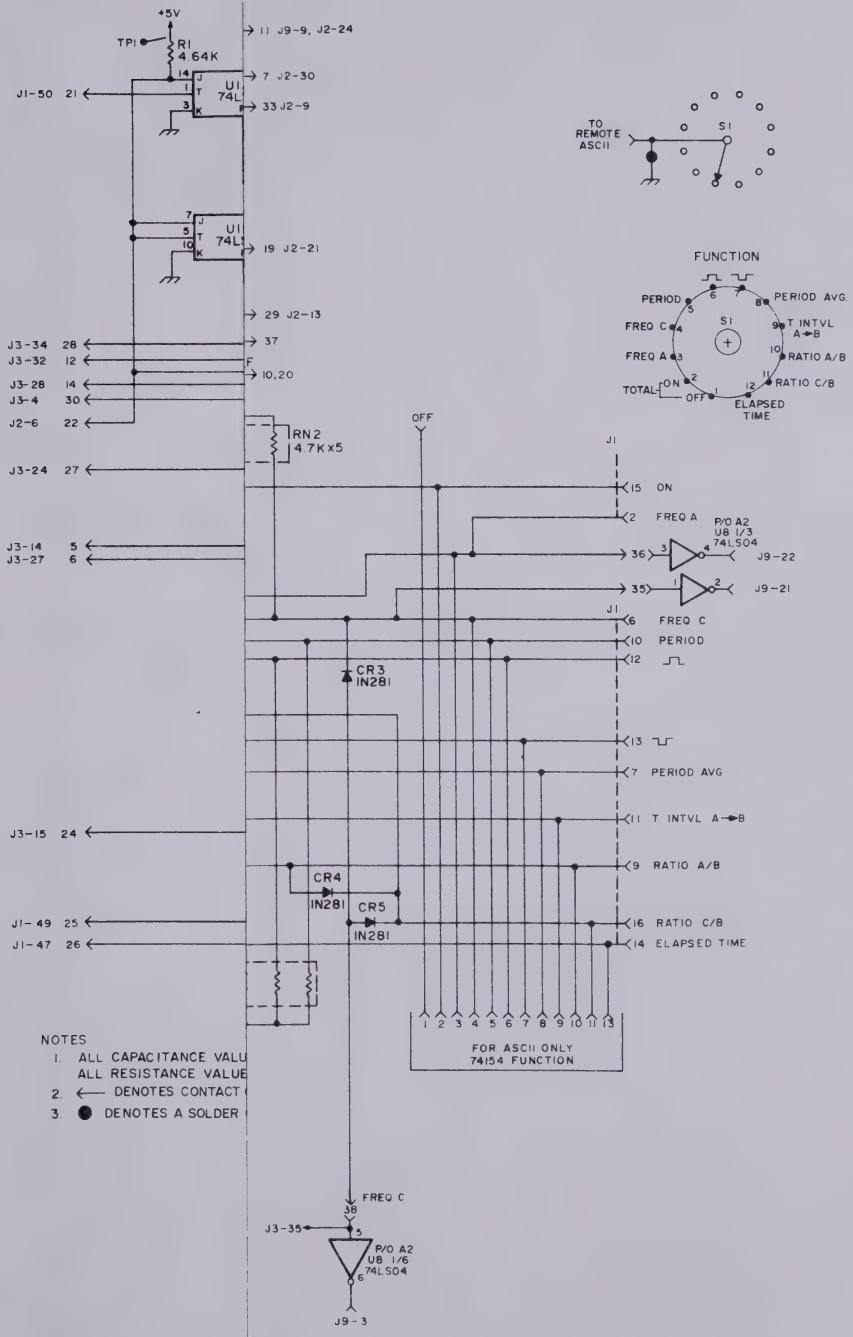



Figure 6-8. Function and Logic Assembly A6, Circuit Diagram

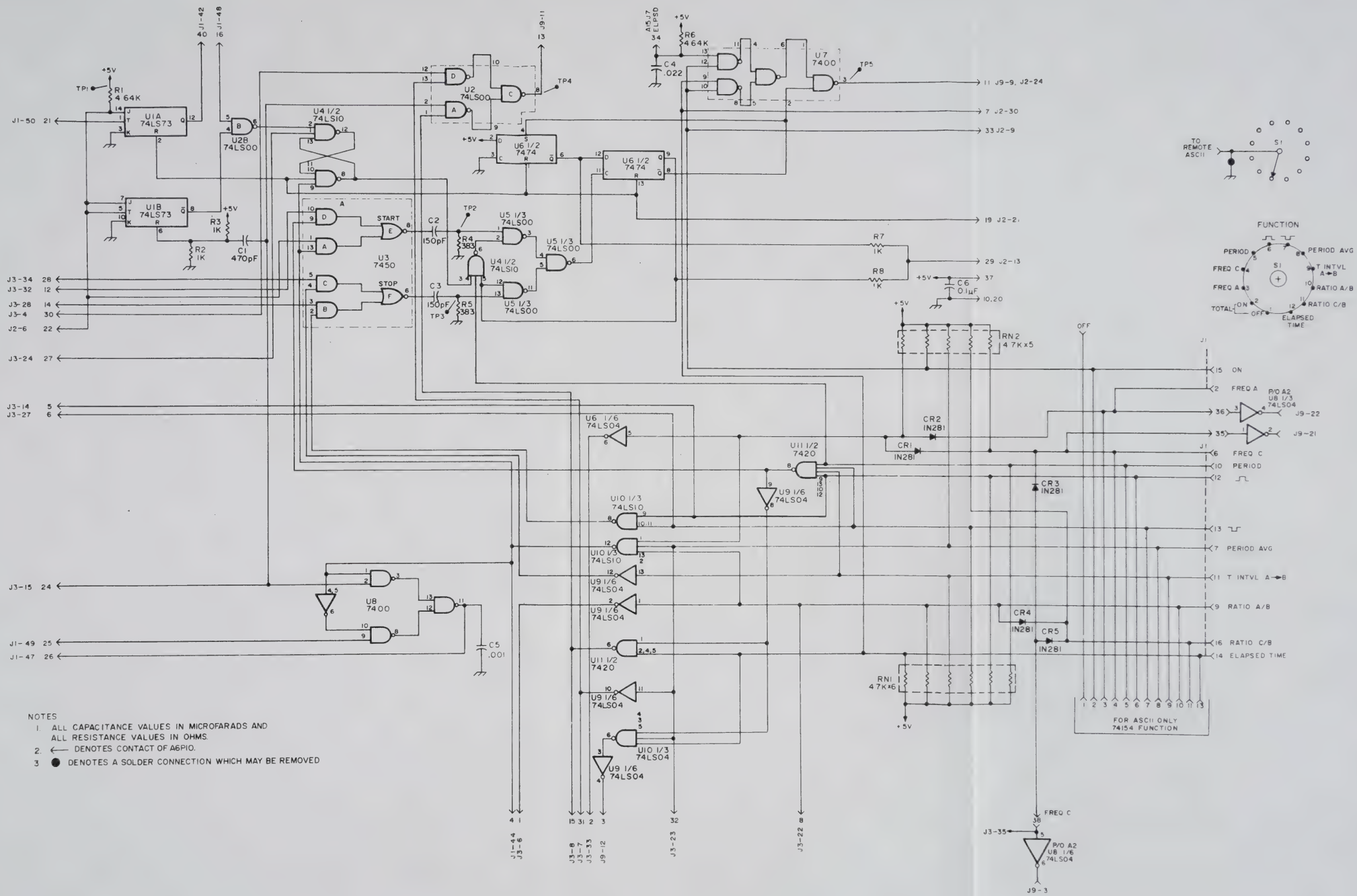



Figure 6-8. Function and Logic Assembly A6, Circuit Diagram

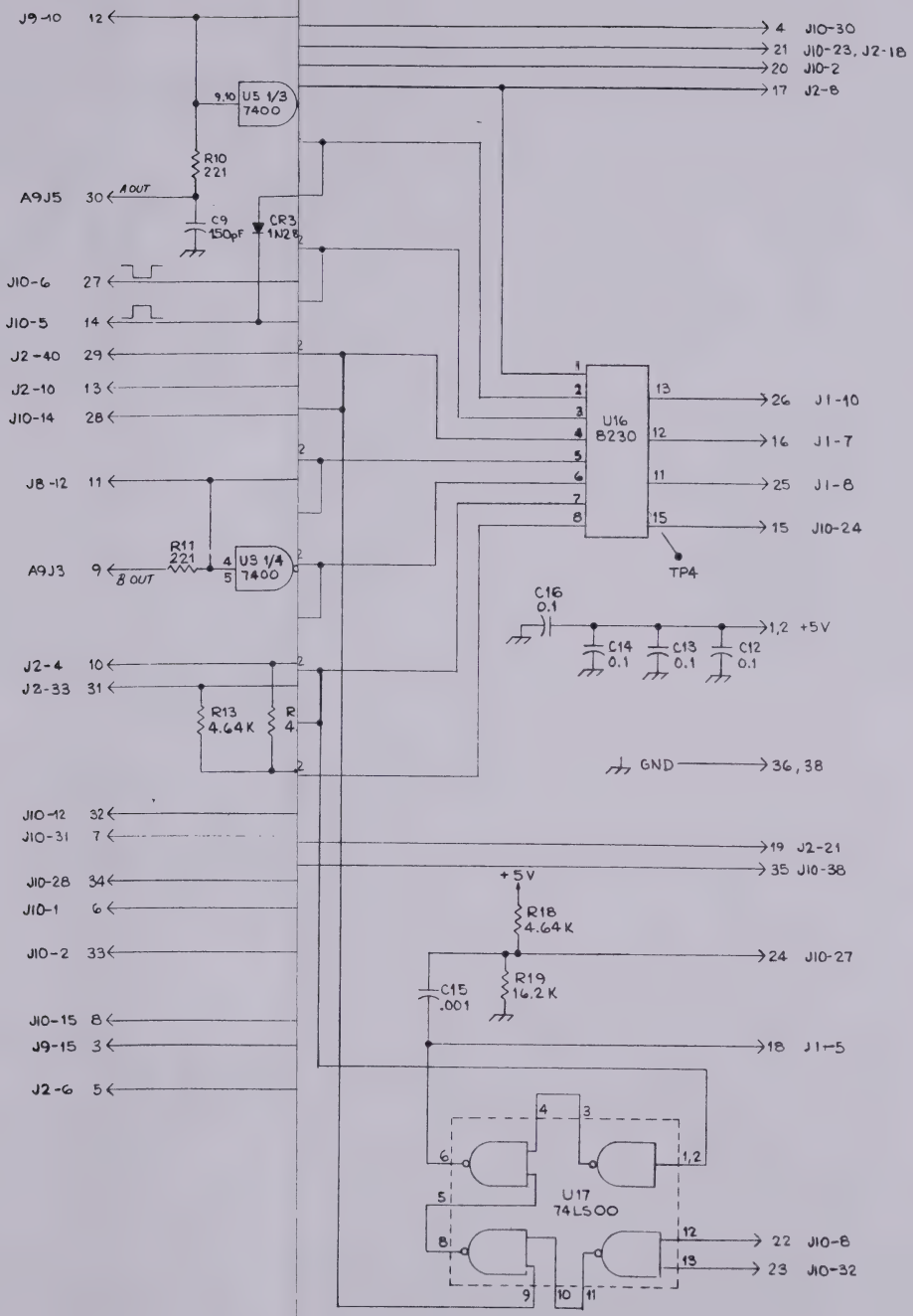
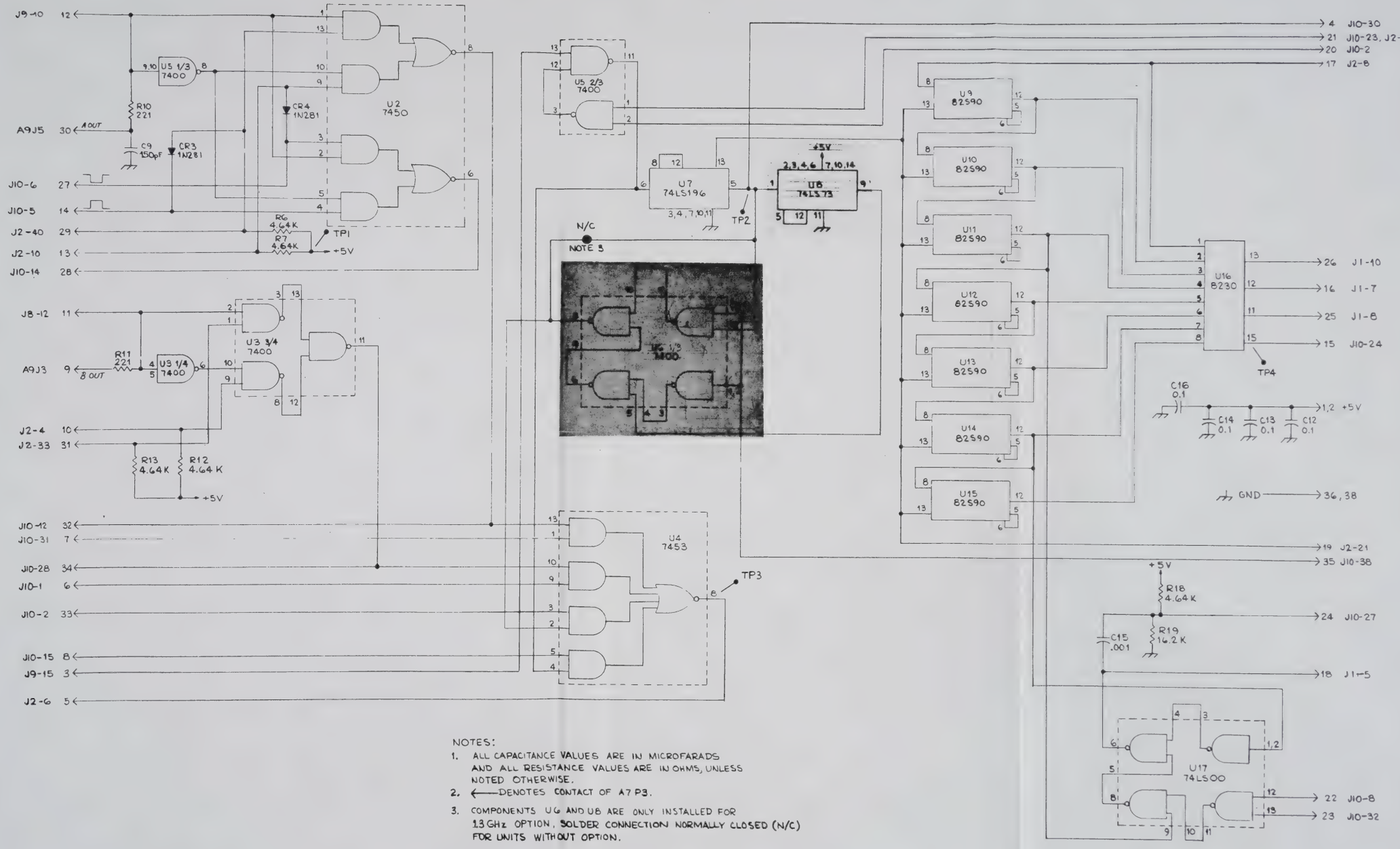



Figure 6-9. Chain Dividers Slope Channel A and B Assembly A7, Circuit Diagram




NOTES:

1. ALL CAPACITANCE VALUES ARE IN MICROFARADS AND ALL RESISTANCE VALUES ARE IN OHMS, UNLESS NOTED OTHERWISE.
2. ⟵ DENOTES CONTACT OF A7 P3.
3. COMPONENTS U6 AND U8 ARE ONLY INSTALLED FOR 1.3 GHz OPTION. SOLDER CONNECTION NORMALLY CLOSED (N/C) FOR UNITS WITHOUT OPTION.

Figure 6-9. Chain Dividers Slope Channel A and B Assembly A7, Circuit Diagram

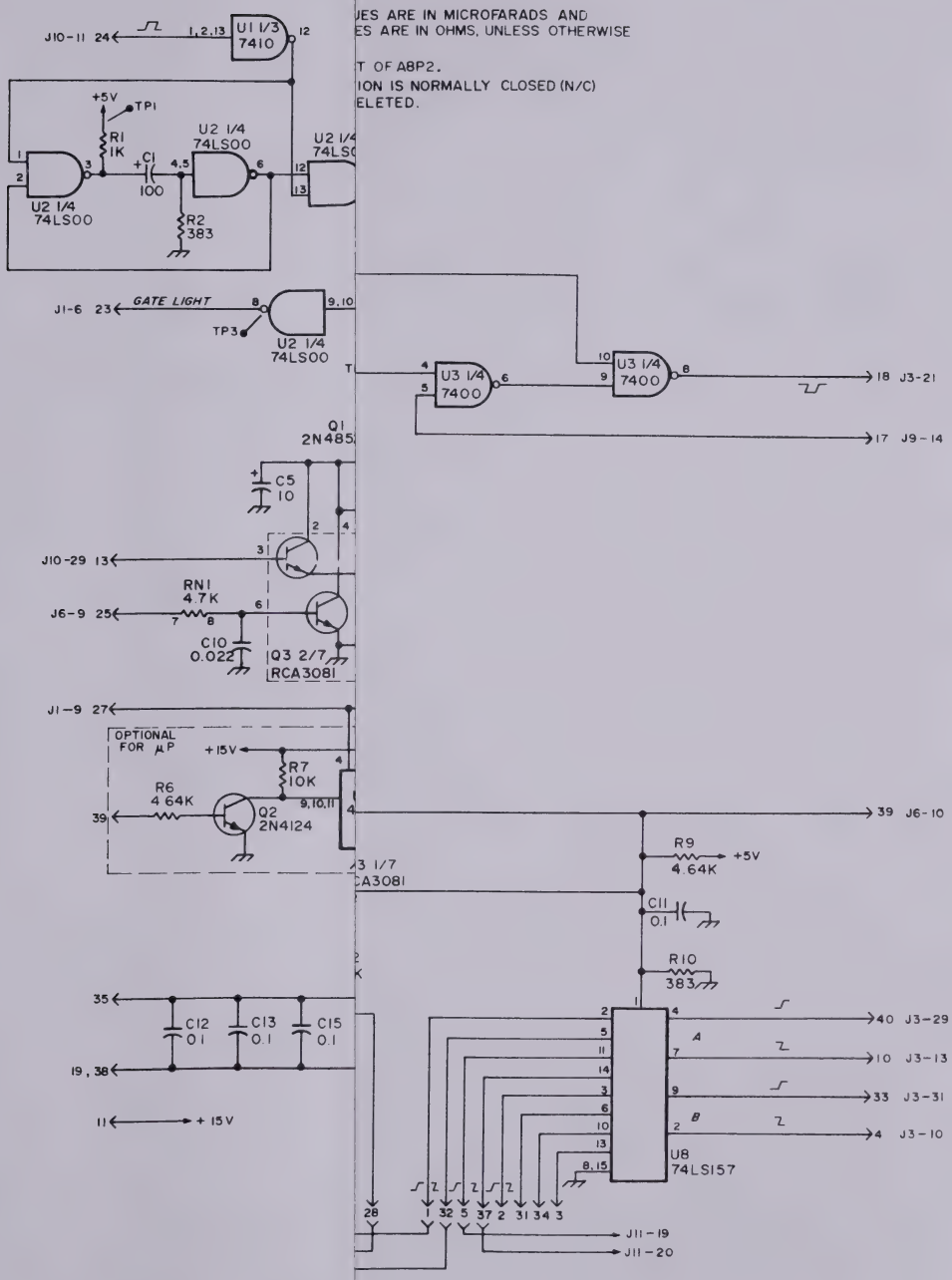



Figure 6-10. Reset, Arming, Burst, Transfer Assembly A8, Circuit Diagram

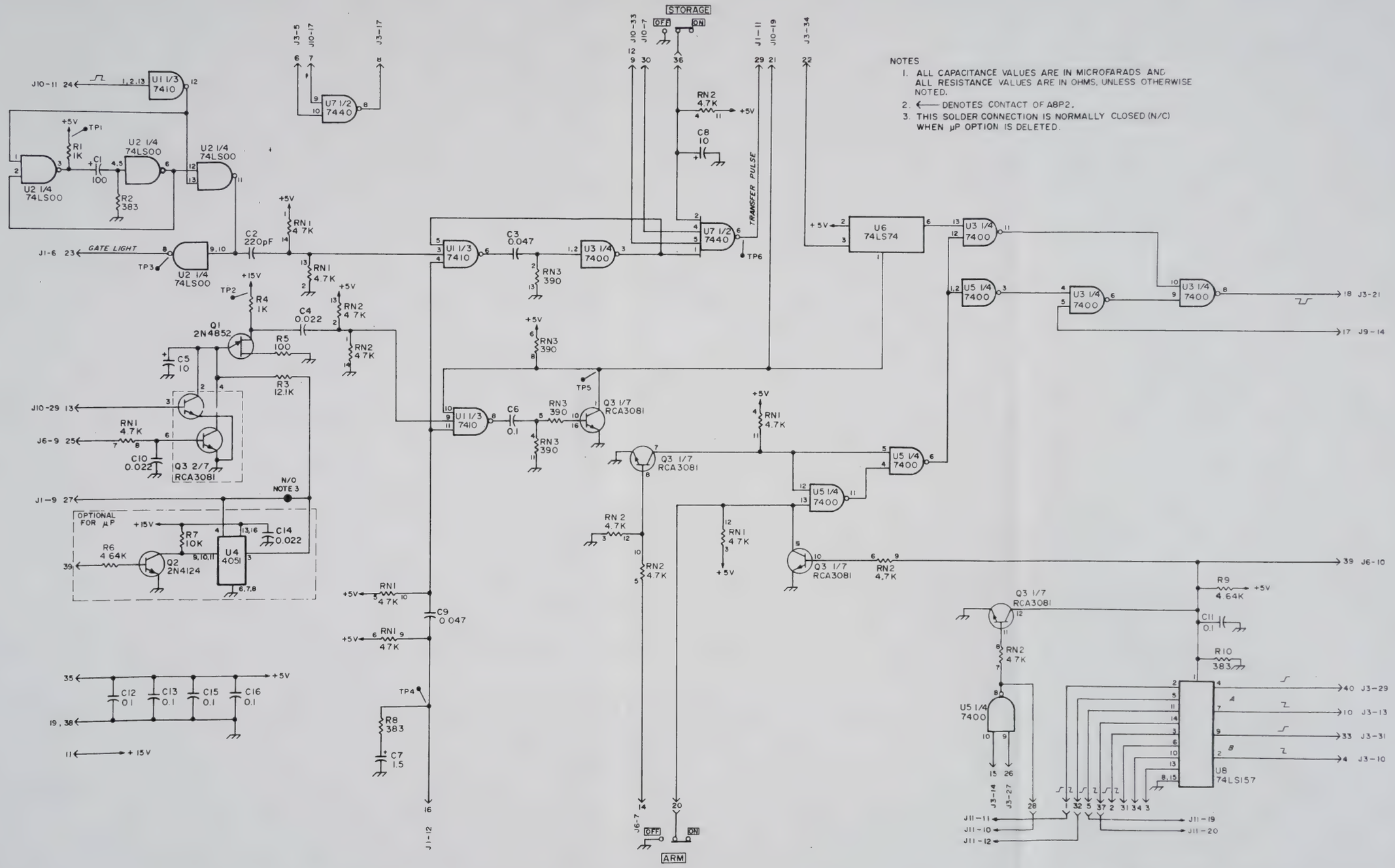



Figure 6-10. Reset, Arming, Burst, Transfer Assembly A8, Circuit Diagram

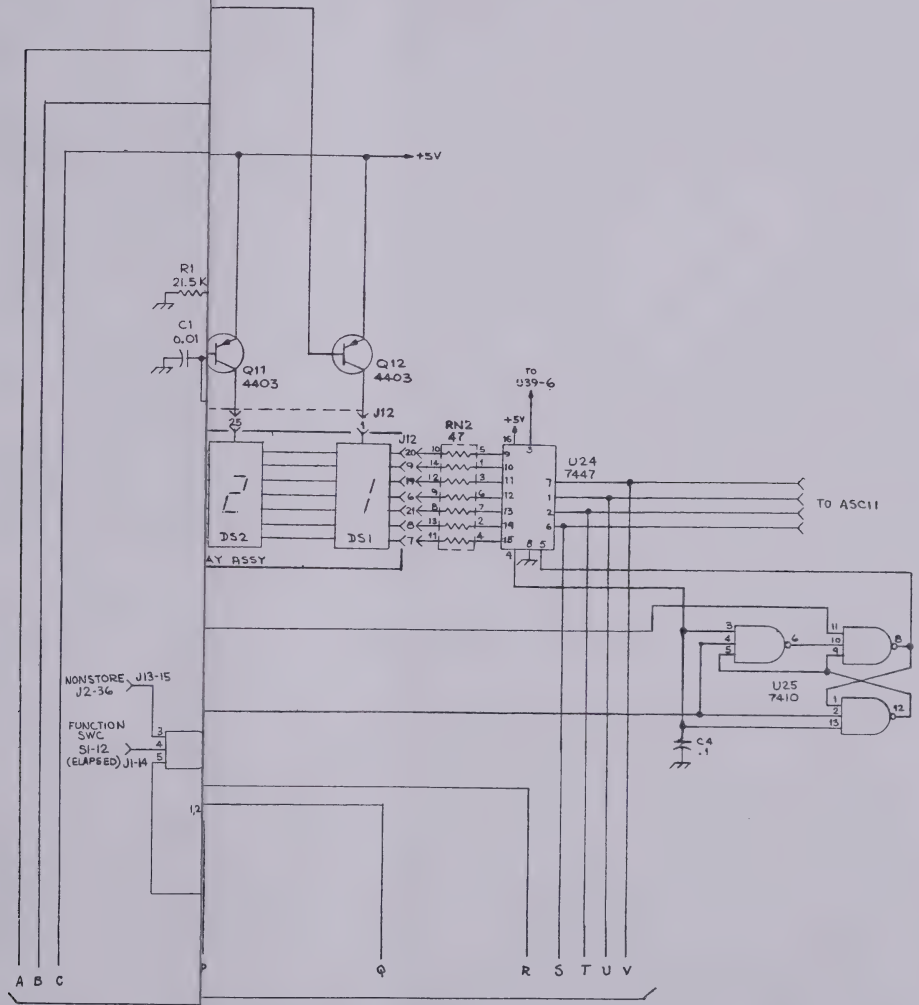



Figure 6-11. Auto and Display Decades Assembly A11, Circuit Diagram (Sheet 1 of 2)

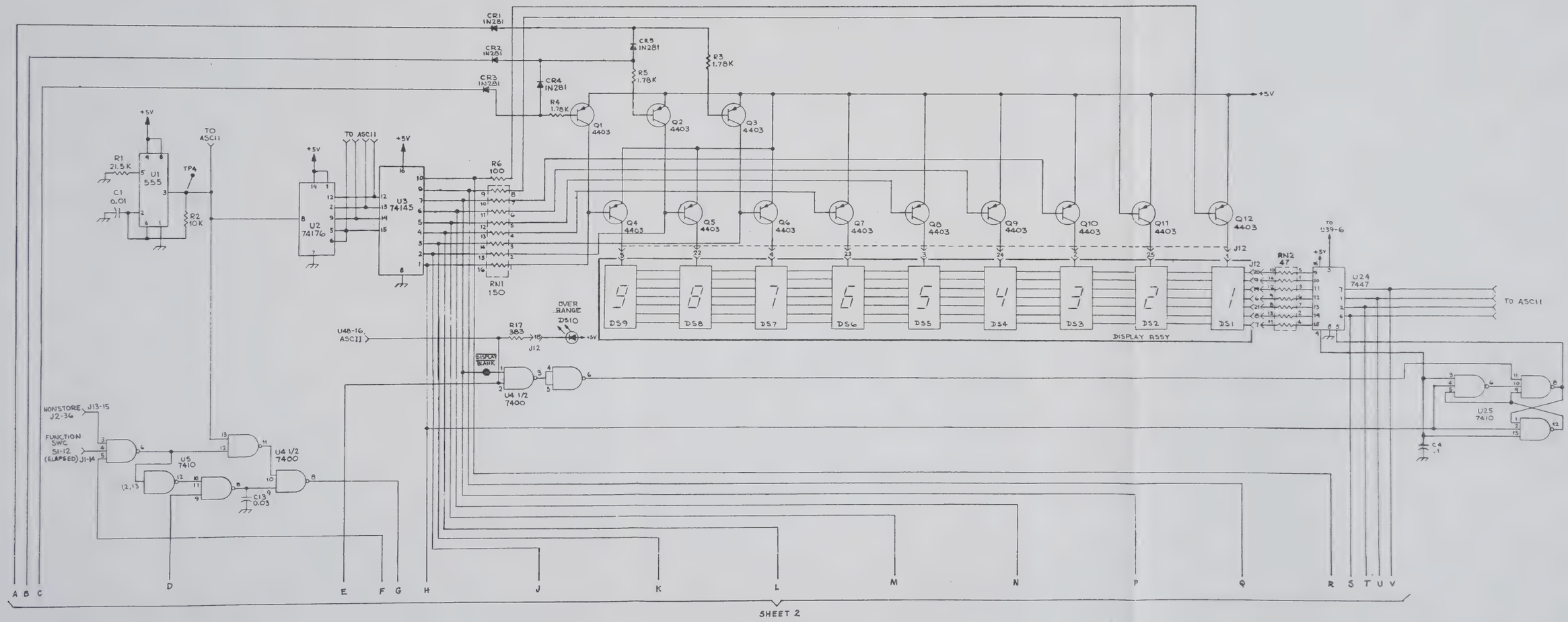



Figure 6-11. Auto and Display Decades Assembly A11, Circuit Diagram (Sheet 1 of 2)

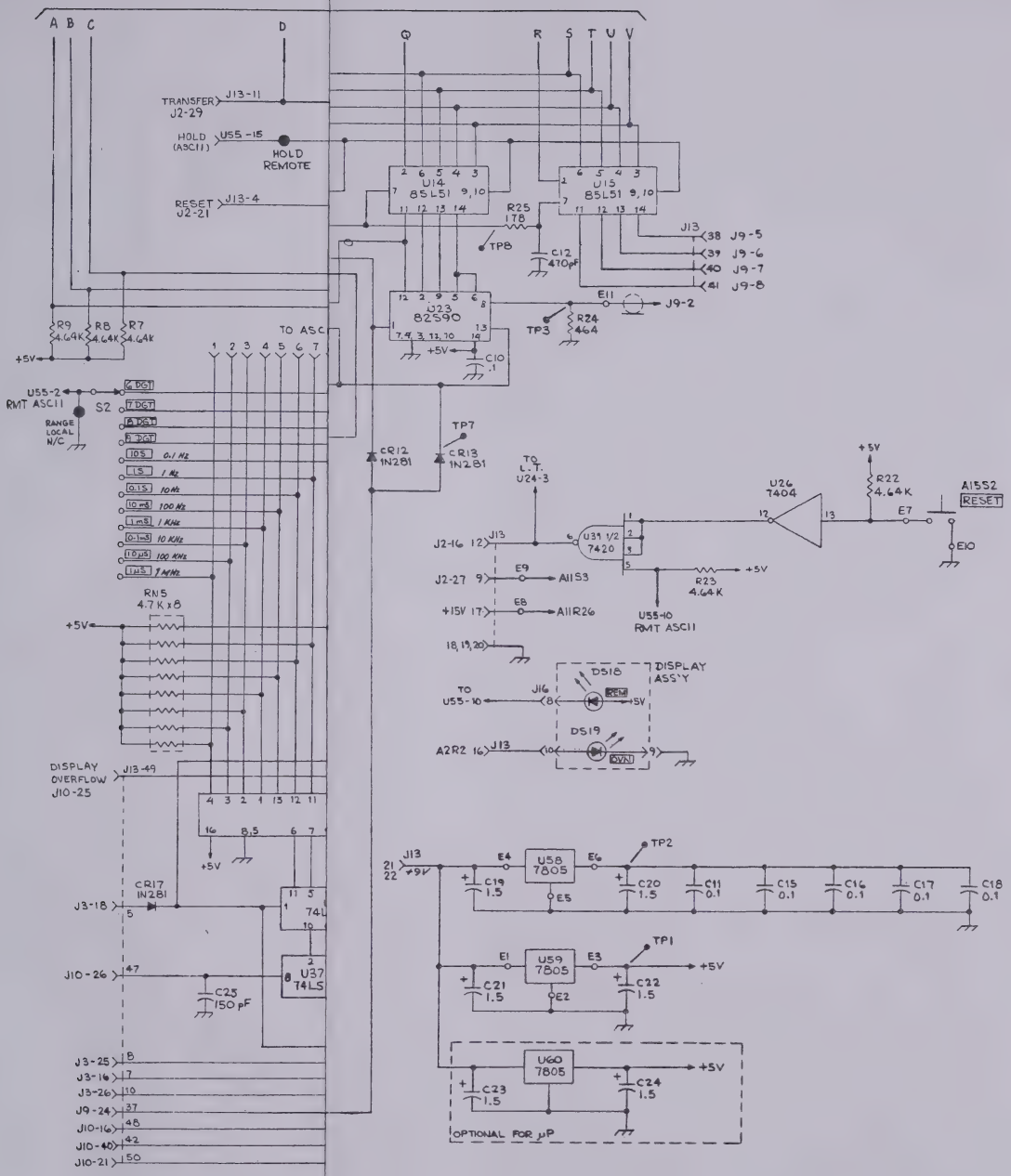



Figure 6-11. Auto and Display Decades Assembly A11, Circuit Diagram (Sheet 2 of 2)

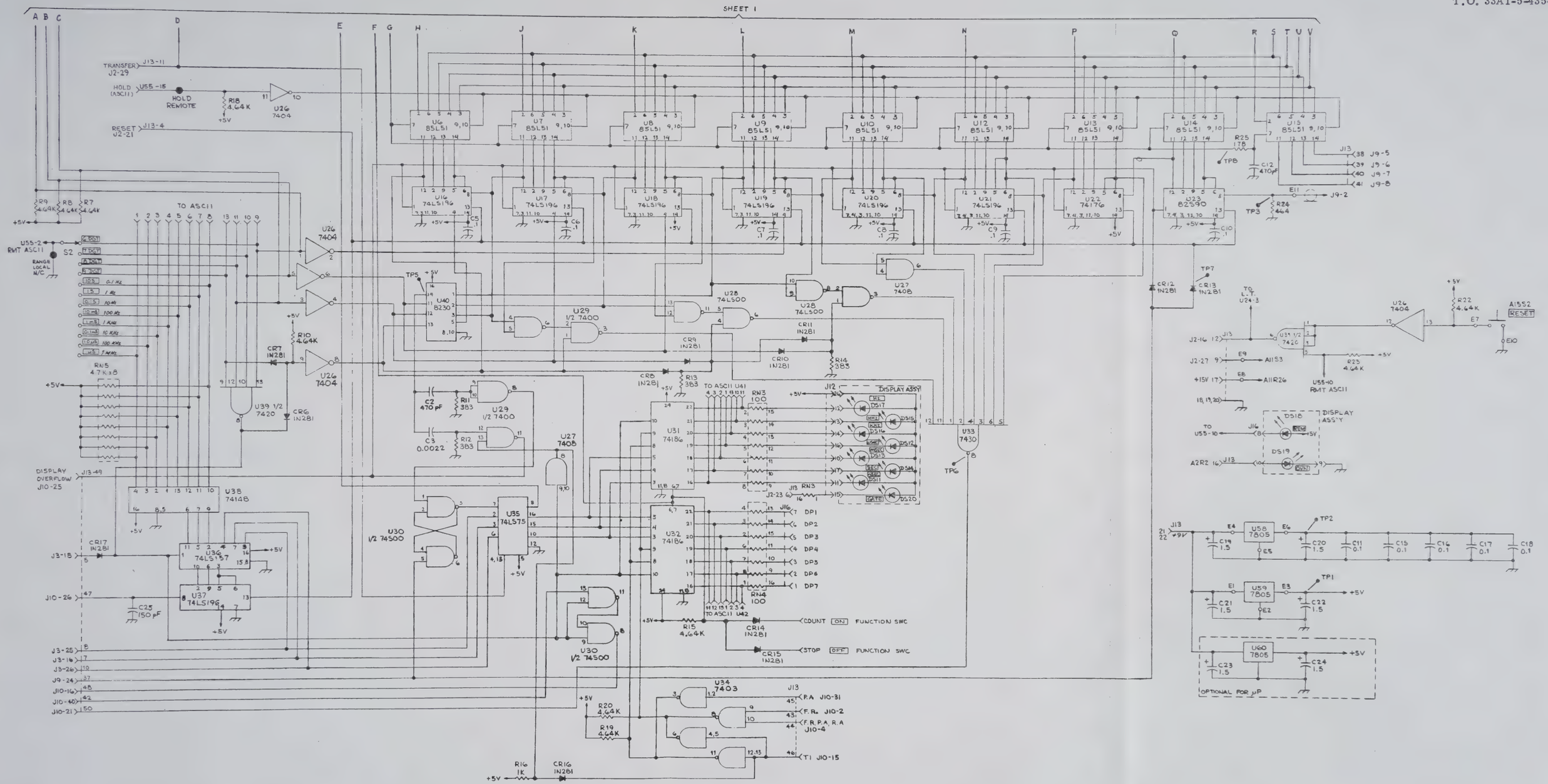



Figure 6-11. Auto and Display Decades Assembly A11, Circuit Diagram (Sheet 2 of 2)

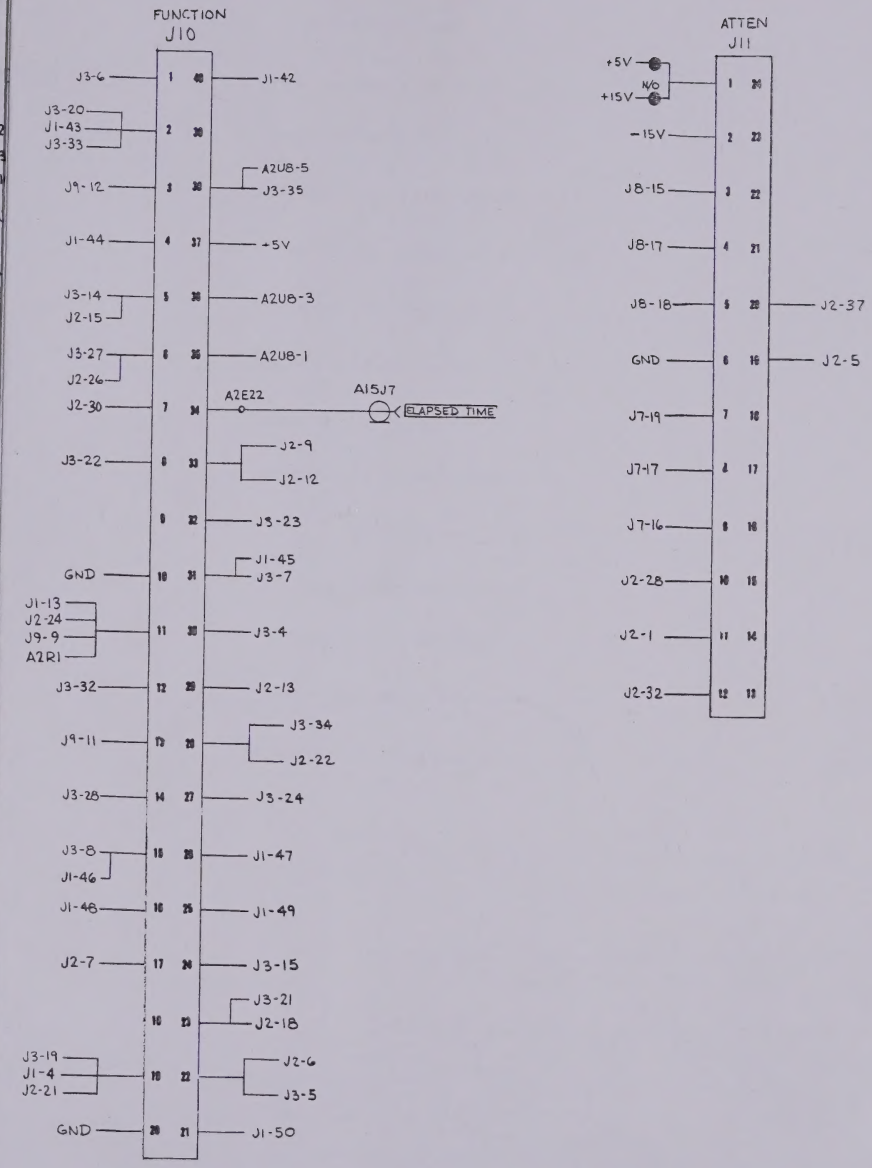



Figure 6-12. Power Supply and Interconnect Assembly A2, Circuit Diagram



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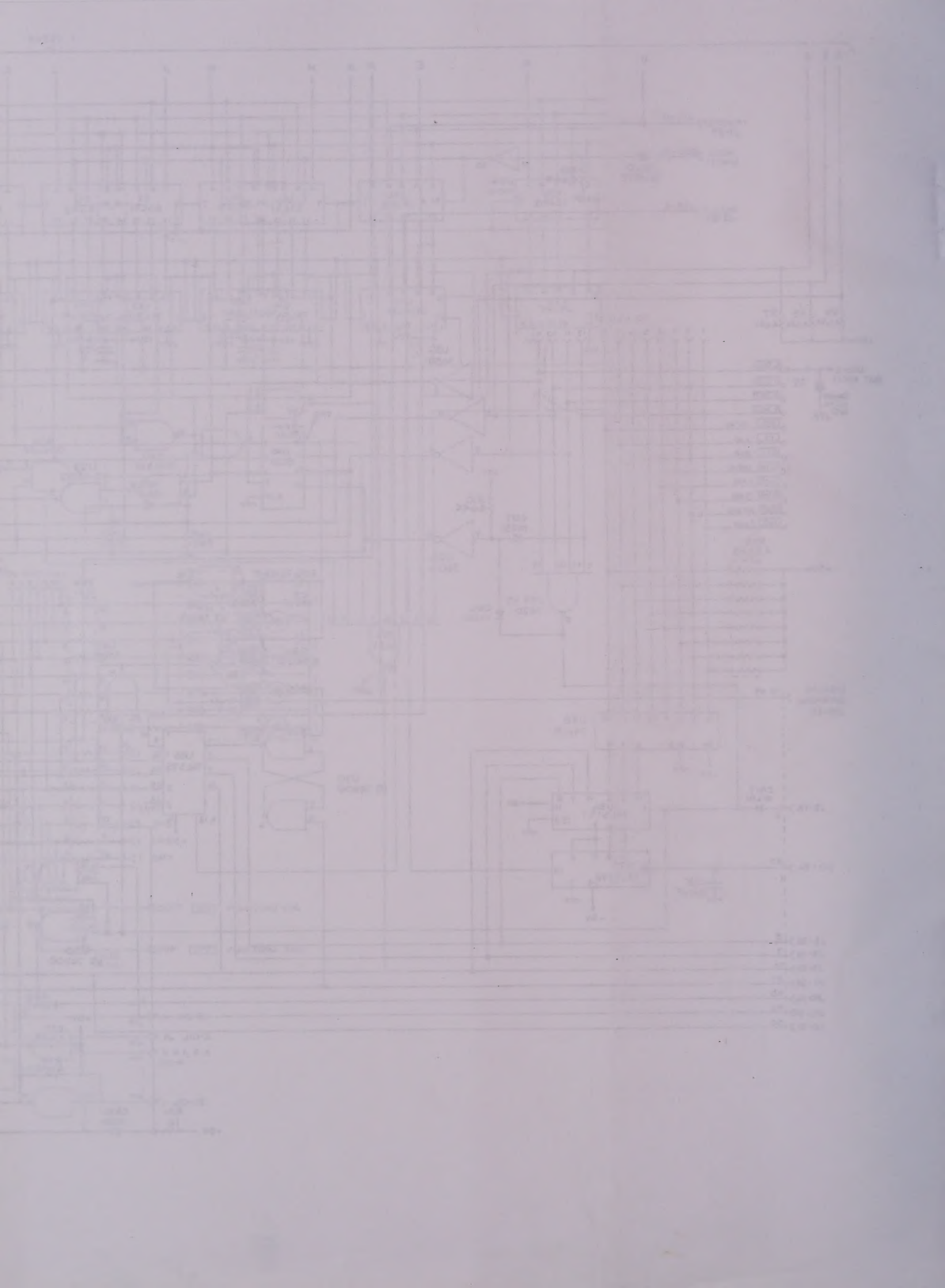

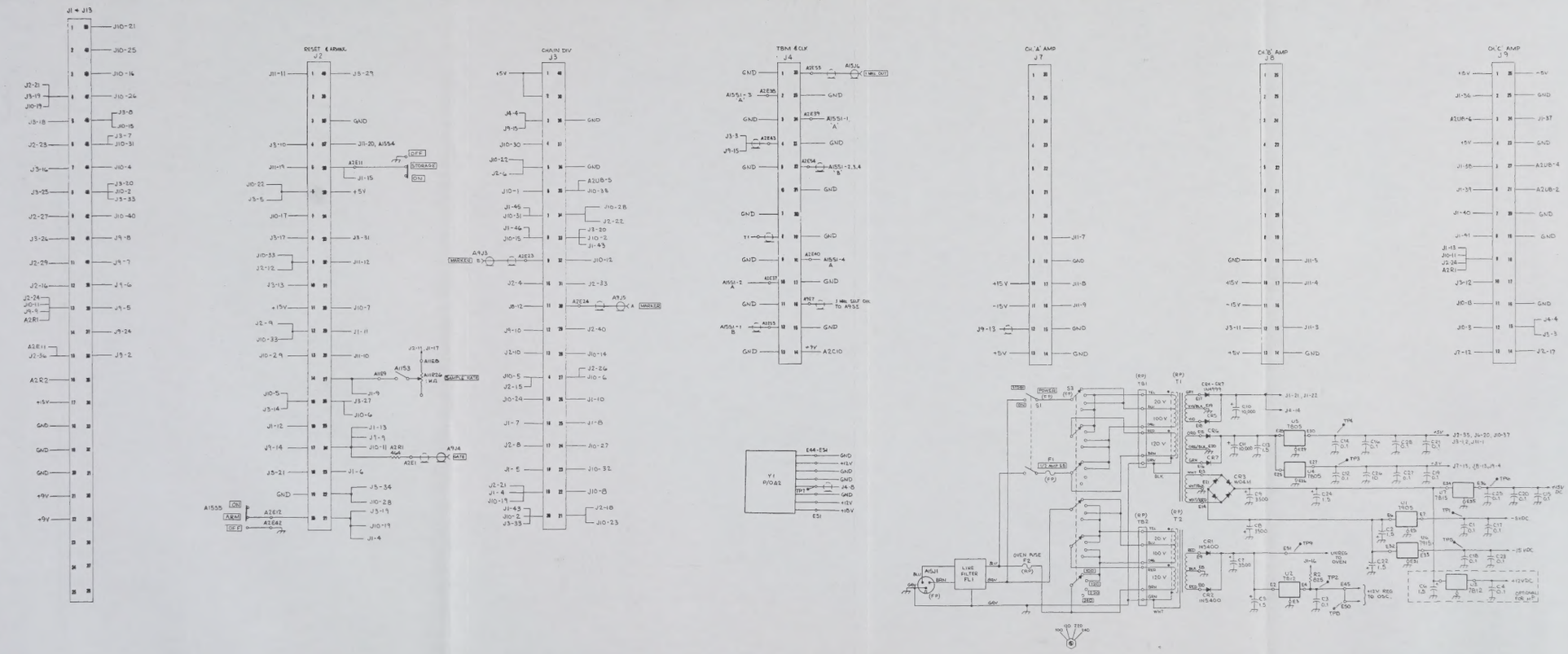


Figure 6-12. Power Supply and Interconnect Assembly A2, Circuit Diagram

6-27/(6-28 Blank)

☆ U.S. GOVERNMENT PRINTING OFFICE: 1979 — 671-150/2782